Figure 136. Maximum Frequency vs. V_{CC}, ATmega169V

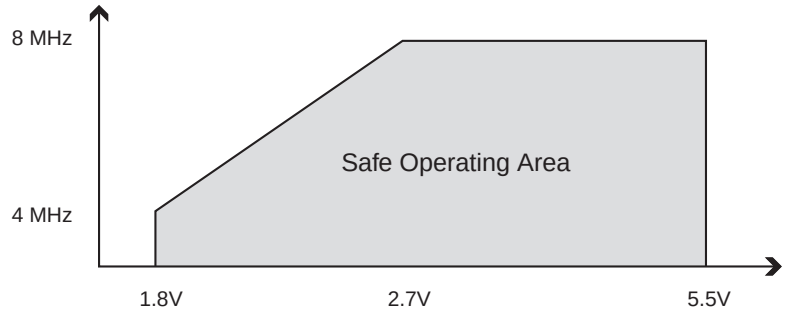
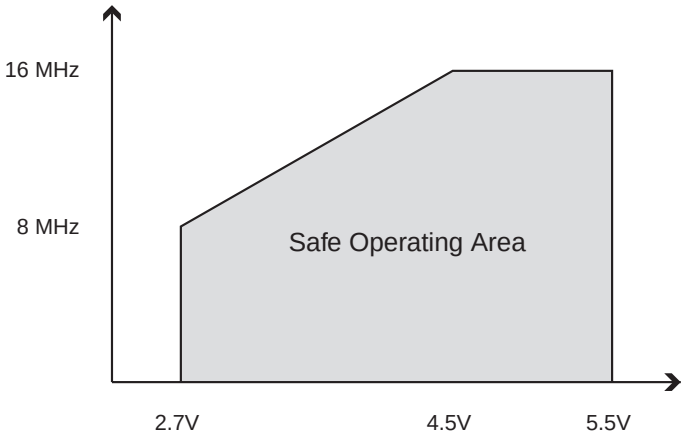


Figure 137. Maximum Frequency vs. V_{CC}, ATmega169



SPI Timing Characteristics

See Figure 138 and Figure 139 for details.

Table 134. SPI Timing Parameters

	Description	Mode	Min	Typ	Max	
1	SCK period	Master		See Table 69		
2	SCK high/low	Master		50% duty cycle		
3	Rise/Fall time	Master		3.6		
4	Setup	Master		10		
5	Hold	Master		10		
6	Out to SCK	Master		$0.5 \cdot t_{sck}$		ns
7	SCK to out	Master		10		
8	SCK to out high	Master		10		
9	$\overline{SS}$ low to out	Slave		15		
10	SCK period	Slave	$4 \cdot t_{ck}$			
11	SCK high/low(1)	Slave	$2 \cdot t_{ck}$			
12	Rise/Fall time	Slave		1.6		µs

Table 134. SPI Timing Parameters

	Description	Mode	Min	Typ	Max	
13	Setup	Slave	10			ns
14	Hold	Slave	t_{ck}			
15	SCK to out	Slave		15		
16	SCK to $\overline{SS}$ high	Slave	20			
17	$\overline{SS}$ high to tri-state	Slave		10		
18	$\overline{SS}$ low to SCK	Slave	20 • t_{ck}			

Note: 1. In SPI Programming mode the minimum SCK high/low period is:
- 2 t_{CLCL} for f_{CK} < 12 MHz
- 3 t_{CLCL} for f_{CK} > 12 MHz

Figure 138. SPI Interface Timing Requirements (Master Mode)

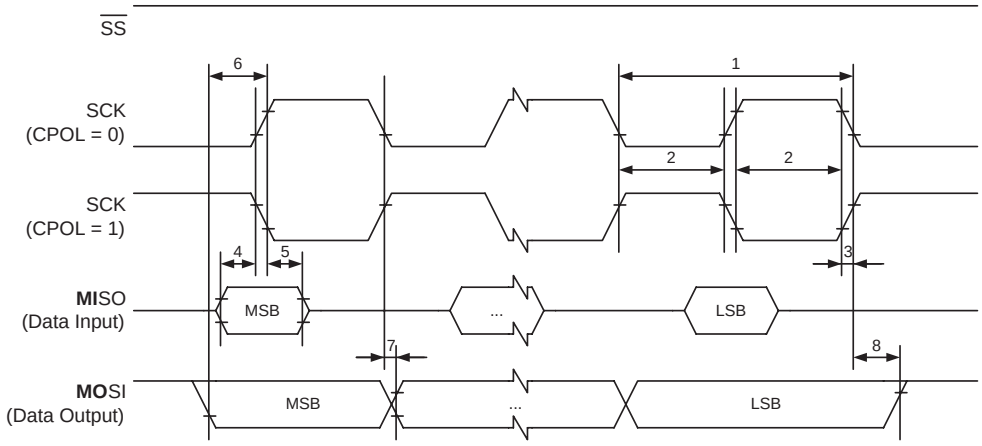
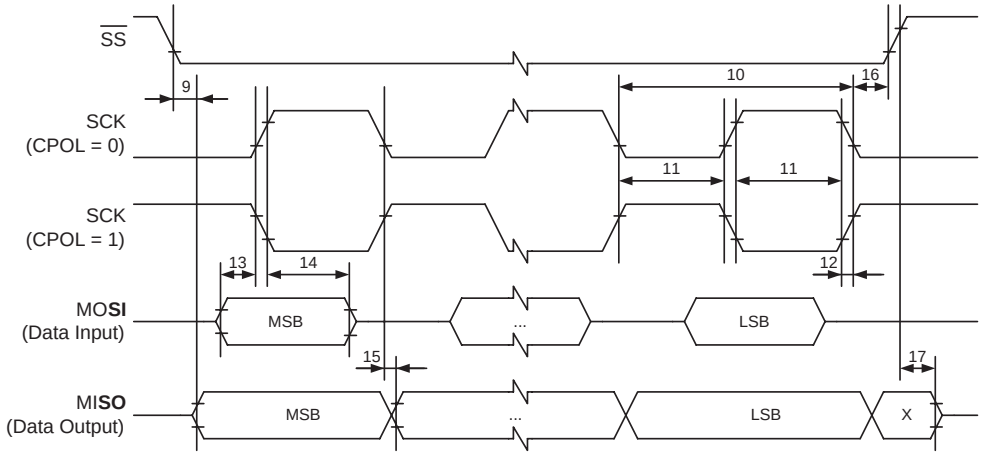


Figure 139. SPI Interface Timing Requirements (Slave Mode)



ADC Characteristics – Preliminary Data

Table 135. ADC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Resolution	Single Ended Conversion		10		Bits
		Differential Conversion		8		Bits
	Absolute accuracy (Including INL, DNL, quantization error, gain and offset error)	Single Ended Conversion V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200 kHz		2	2.5	LSB
		Single Ended Conversion V_{REF} = 4V, V_{CC} = 4V, ADC clock = 1 MHz		4.5		LSB
		Single Ended Conversion V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200 kHz Noise Reduction Mode		2		LSB
		Single Ended Conversion V_{REF} = 4V, V_{CC} = 4V, ADC clock = 1 MHz Noise Reduction Mode		4.5		LSB
	Integral Non-Linearity (INL)	Single Ended Conversion V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200 kHz		0.5		LSB
	Differential Non-Linearity (DNL)	Single Ended Conversion V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200 kHz		0.25		LSB
	Gain Error	Single Ended Conversion V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200 kHz		2		LSB
	Offset Error	Single Ended Conversion V_{REF} = 4V, V_{CC} = 4V, ADC clock = 200 kHz		2		LSB
	Conversion Time	Free Running Conversion	13		260	µs
	Clock Frequency	Single Ended Conversion	50		1000	kHz
AVCC	Analog Supply Voltage		V_{CC} - 0.3		V_{CC} + 0.3	V
V_{REF}	Reference Voltage	Single Ended Conversion	1.0		AVCC	V
		Differential Conversion	1.0		AVCC - 0.5	V
V_{IN}	Input Voltage	Single ended channels	GND		V_{REF}	V
		Differential Conversion	0		AVCC[1]	V
	Input Bandwidth	Single Ended Channels		38,5		kHz
		Differential Channels		4		kHz
V_{INT}	Internal Voltage Reference		1.0	1.1	1.2	V
R_{REF}	Reference Input Resistance			32		kΩ
R_{AIN}	Analog Input Resistance			100		MΩ

Note: 1. V_{DIFF} must be below V_{REF}

LCD Controller Characteristics – Preliminary Data

Table 136. LCD Controller Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LCD}	LCD Driver Current	Total for All COM and SEG pins		100		µA
R_{LCD}	LCD Driver Output Resistance	Per COM or SEG pin		10		kΩ

ATmega169 Typical Characteristics

The following charts show typical behavior. These figures are not tested during manufacturing. All current consumption measurements are performed with all I/O pins configured as inputs and with internal pull-ups enabled. A sine wave generator with rail-to-rail output is used as clock source.

All Active- and Idle current consumption measurements are done with all bits in the PRR register set and thus, the corresponding I/O modules are turned off. Also the Analog Comparator is disabled during these measurements. Table 137 and Table 138 on page 310 show the additional current consumption compared to I_{CC} Active and I_{CC} Idle for every I/O module controlled by the Power Reduction Register. See “Power Reduction Register” on page 34 for details.

The power consumption in Power-down mode is independent of clock selection.

The current consumption is a function of several factors such as: operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, code executed and ambient temperature. The dominating factors are operating voltage and frequency.

The current drawn from capacitive loaded pins may be estimated (for one pin) as $C_L*V_{CC}*f$ where C_L = load capacitance, V_{CC} = operating voltage and f = average switching frequency of I/O pin.

The parts are characterized at frequencies higher than test limits. Parts are not guaranteed to function properly at frequencies higher than the ordering code indicates.

The difference between current consumption in Power-down mode with Watchdog Timer enabled and Power-down mode with Watchdog Timer disabled represents the differential current drawn by the Watchdog Timer.

Active Supply Current

Figure 140. Active Supply Current vs. Frequency (0.1 - 1.0 MHz)

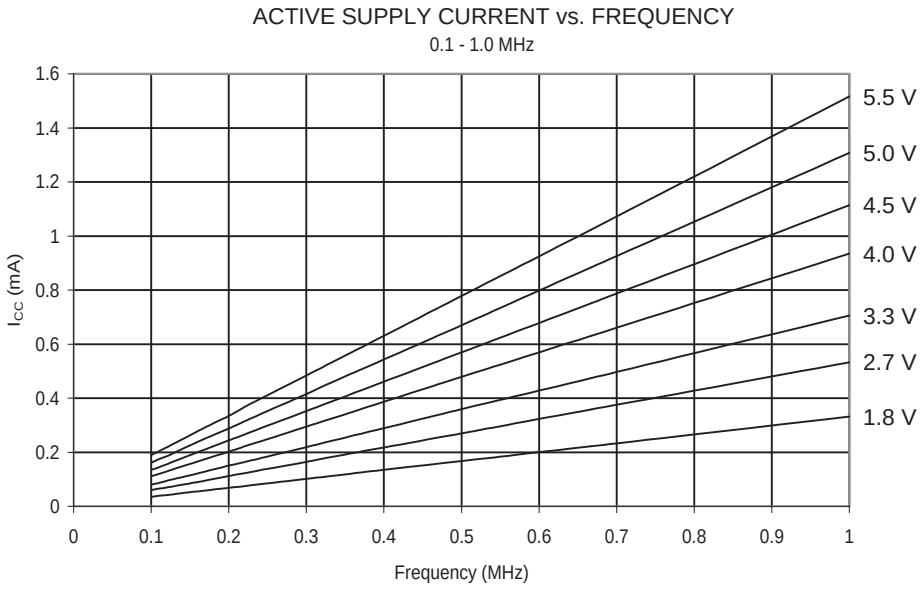


Figure 141. Active Supply Current vs. Frequency (1 - 20 MHz)

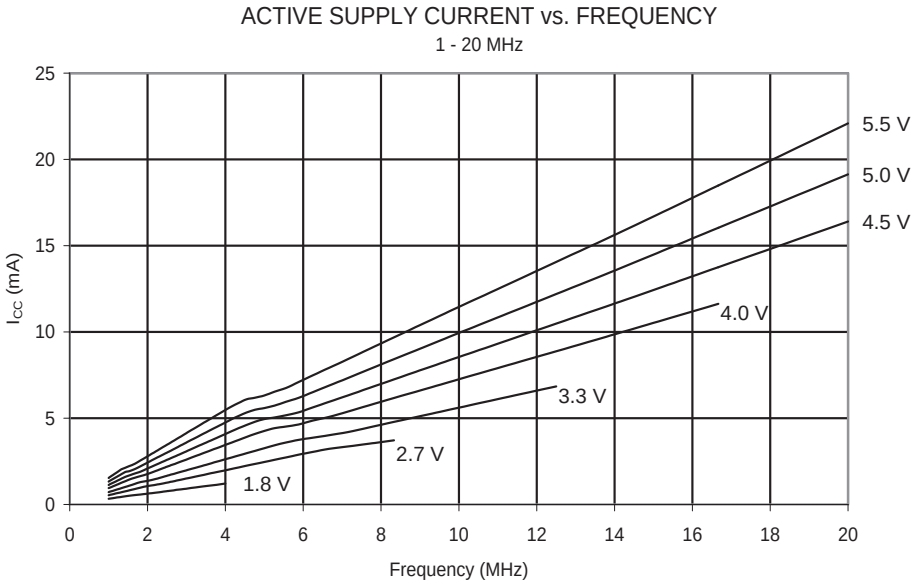


Figure 142. Active Supply Current vs. V_{CC} (Internal RC Oscillator, 8 MHz

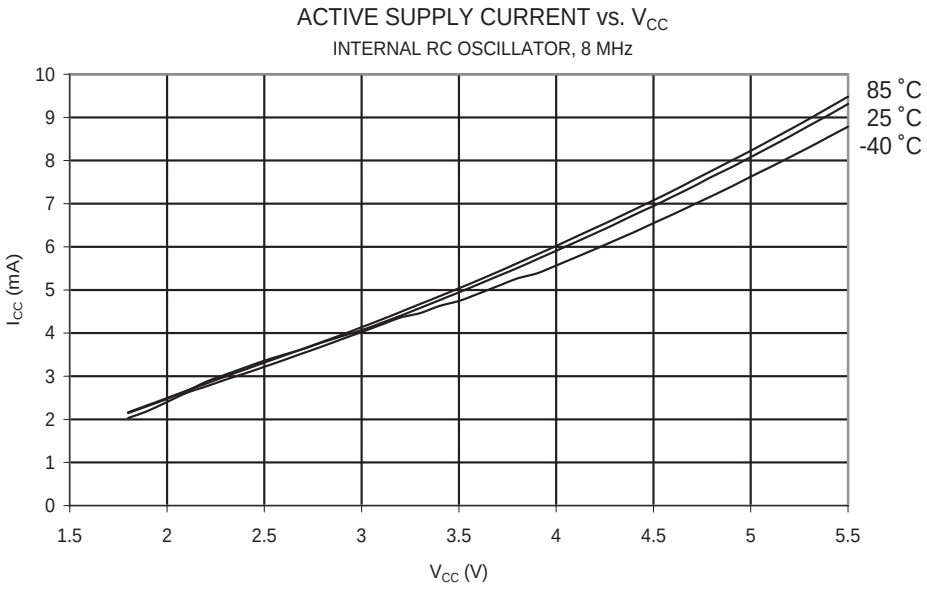


Figure 143. Active Supply Current vs. V_{CC} (Internal RC Oscillator, 1 MHz)

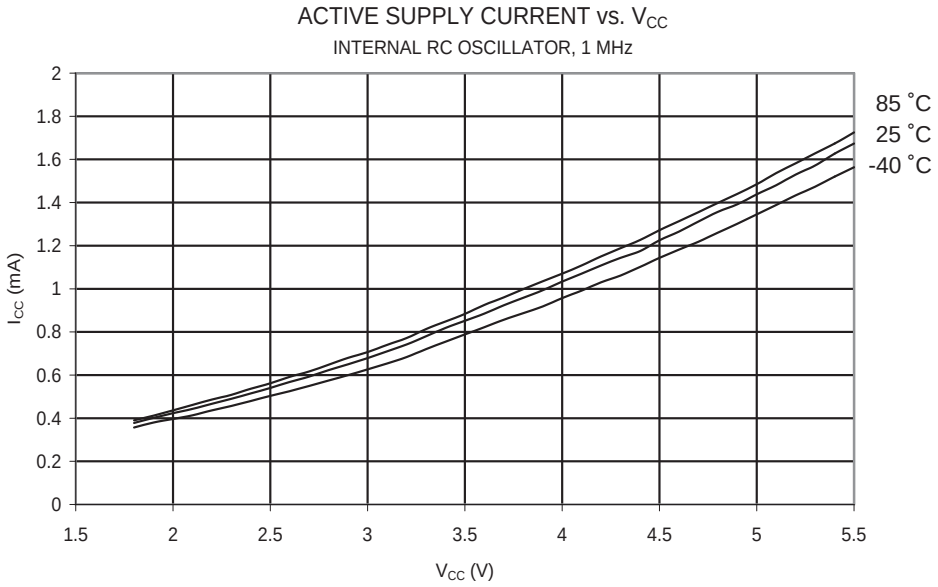
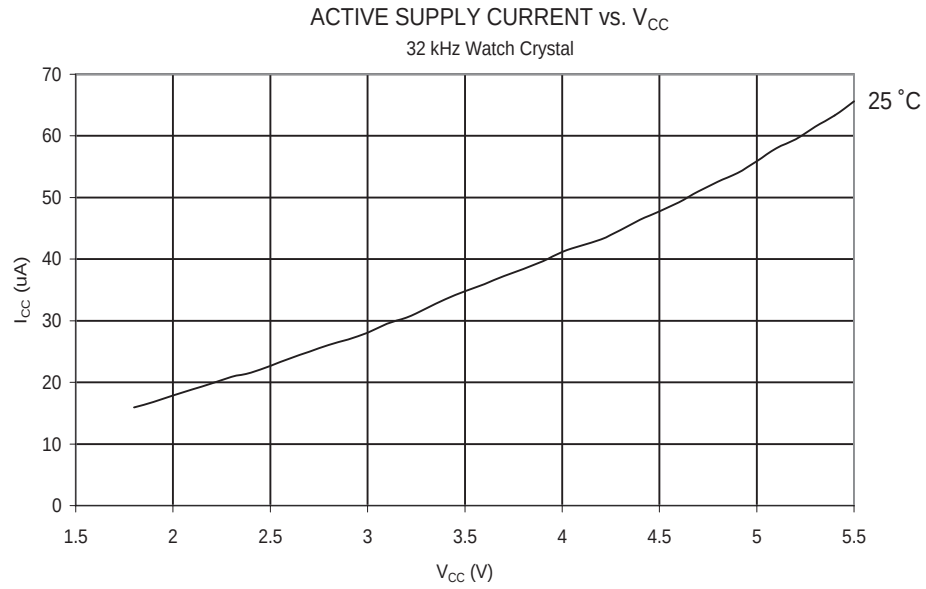


Figure 144. Active Supply Current vs. V_{CC} (32 kHz Watch Crystal)



Idle Supply Current

Figure 145. Idle Supply Current vs. Frequency (0.1 - 1.0 MHz)

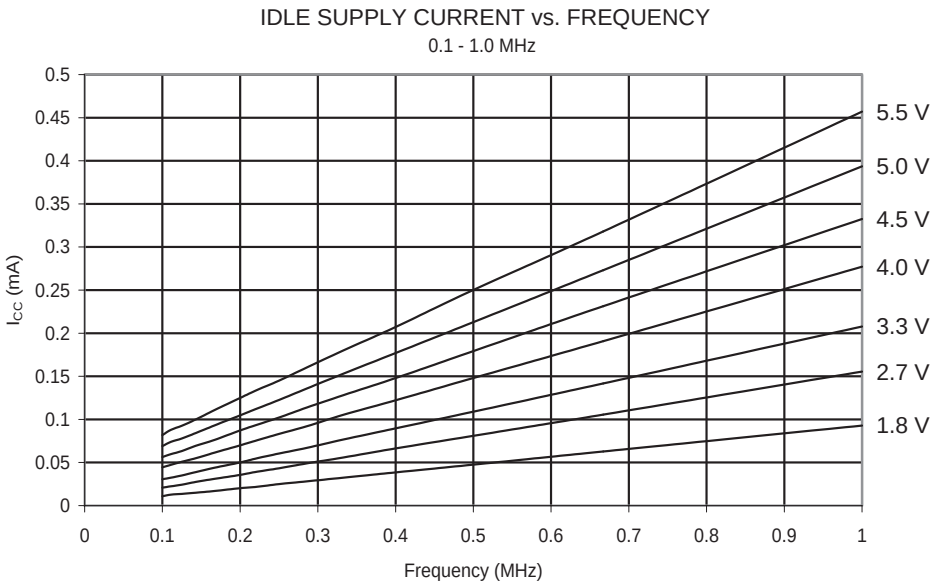


Figure 146. Idle Supply Current vs. Frequency (1 - 20 MHz)

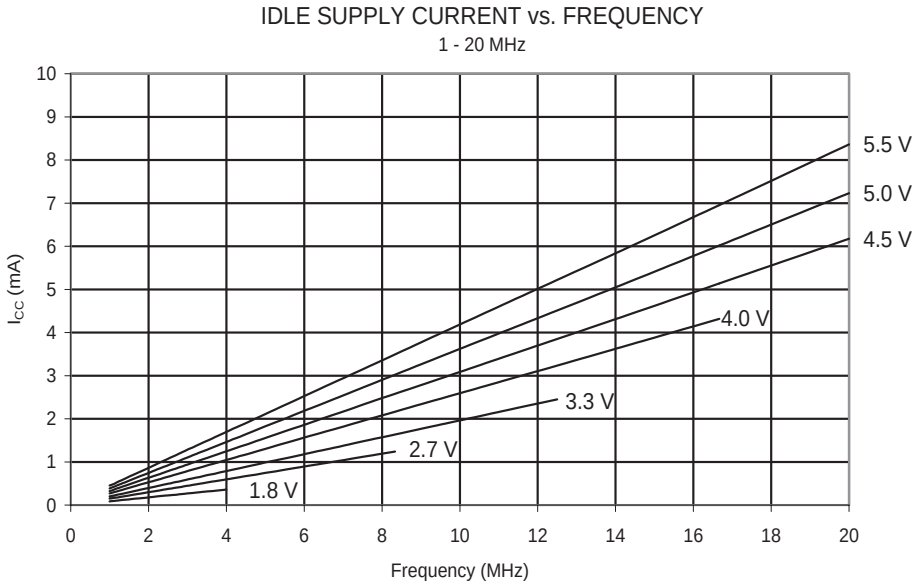


Figure 147. Idle Supply Current vs. V_{CC} (Internal RC Oscillator, 8 MHz)

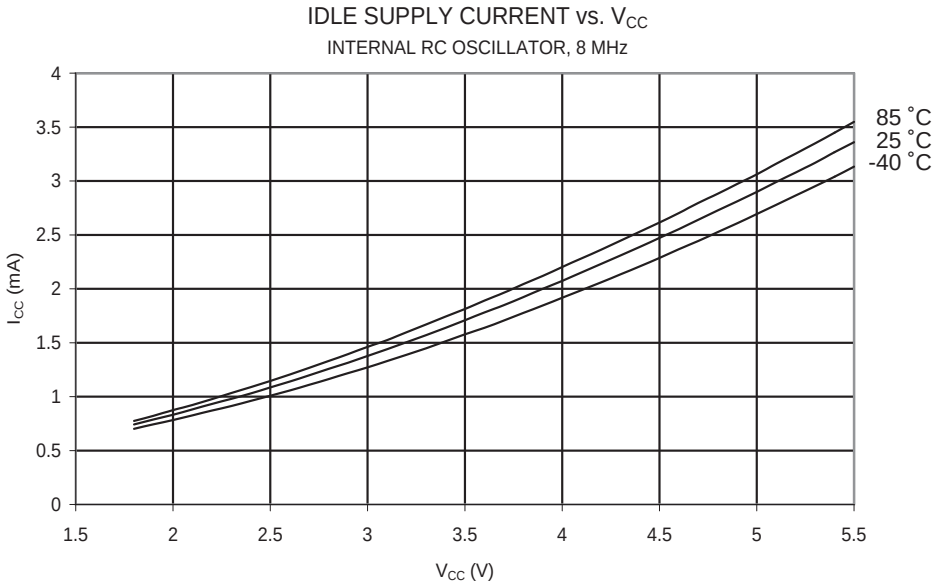


Figure 148. Idle Supply Current vs. V_{CC} (Internal RC Oscillator, 1 MHz)

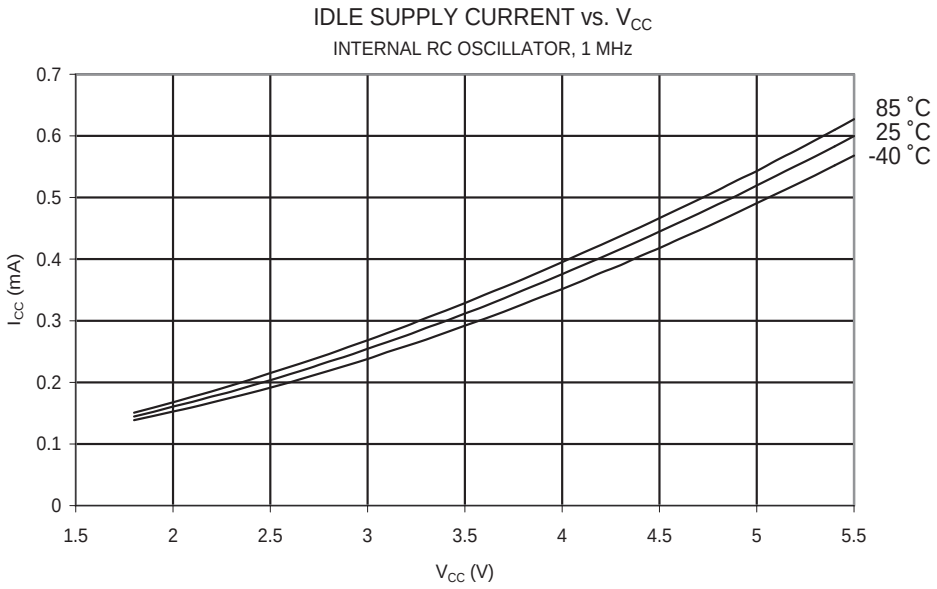
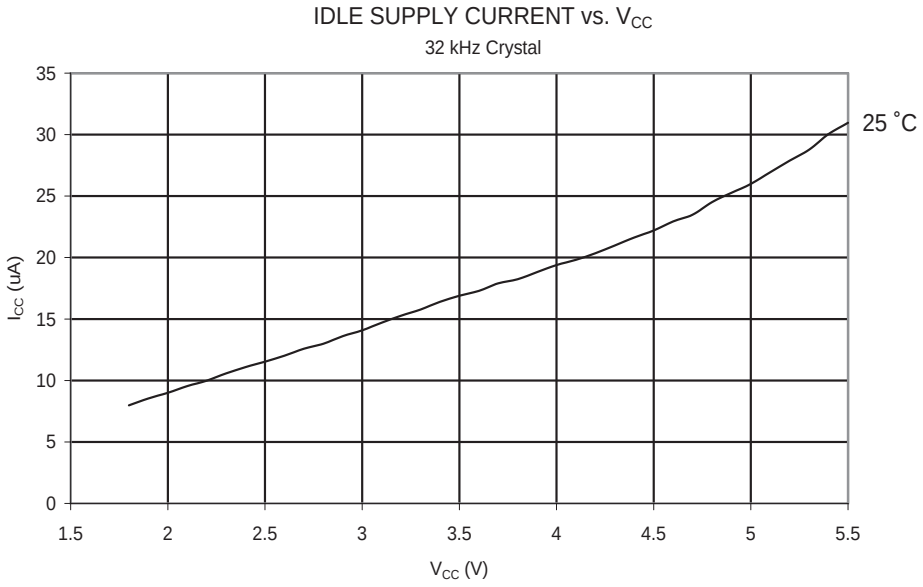


Figure 149. Idle Supply Current vs. V_{CC} (32 kHz Crystal)



Supply Current of I/O modules

The tables and formulas below can be used to calculate the additional current consumption for the different I/O modules in Active and Idle mode. The enabling or disabling of the I/O modules are controlled by the Power Reduction Register. See “Power Reduction Register” on page 34 for details.

Table 137.
Additional Current Consumption for the different I/O modules (absolute values)

PRR bit	Typical numbers		
	V_{CC} = 2V, F = 1MHz	V_{CC} = 3V, F = 4MHz	V_{CC} = 5V, F = 8MHz
PRADC	18 µA	116 µA	495 µA
PRUSART0	11µA	79 µA	313 µA
PRSPI	10 µA	72 µA	283 µA
PRTIM1	19 µA	117 µA	481 µA
PRLCD	19 µA	124 µA	531 µA

Table 138.
Additional Current Consumption (percentage) in Active and Idle mode

PRR bit	Additional Current consumption compared to Active with external clock (see Figure 140 and Figure 141)	Additional Current consumption compared to Idle with external clock (see Figure 145 and Figure 146)
PRADC	5.6%	18.7%
PRUSART0	3.7%	12.4%
PRSPI	3.2%	10.8%
PRTIM1	5.6%	18.6%
PRLCD	5.9%	19.9%

It is possible to calculate the typical current consumption based on the numbers from Table 138 for other V_{CC} and frequency settings than listed in Table 137.

Example 1

Calculate the expected current consumption in idle mode with USART0, TIMER1, and SPI enabled at V_{CC} = 3.0V and F = 1MHz. From Table 138, second column, we see that we need to add 12.4% for the USART0, 10.8% for the SPI, and 18.6% for the TIMER1 module. Reading from Figure 145, we find that the idle current consumption is ~0.18mA at V_{CC} = 3.0V and F = 1MHz. The total current consumption in idle mode with USART0, TIMER1, and SPI enabled, gives:

$$I_{CCtotal} \approx 0.18mA \bullet (1 + 0.124 + 0.108 + 0.186) \approx 0.26mA$$

Example 2

Same conditions as in example 1, but in active mode instead. From Table 138, second column we see that we need to add 3.7% for the USART0, 3.2% for the SPI, and 5.6% for the TIMER1 module. Reading from Figure 140, we find that the active current consumption is ~0.6mA at V_{CC} = 3.0V and F = 1MHz. The total current consumption in idle mode with USART0, TIMER1, and SPI enabled, gives:

$$I_{CCtotal} \approx 0.6mA \bullet (1 + 0.037 + 0.032 + 0.056) \approx 0.68mA$$

Example 3

All I/O modules should be enabled. Calculate the expected current consumption in active mode at V_{CC} = 3.3V and F = 10MHz. We find the active current consumption without the I/O modules to be ~ 5.6mA (from Figure 141). Then, by using the numbers from Table 138 - first column, we find the total current consumption:

$$I_{CCtotal} \approx 5.6mA \bullet (1 + 0.056 + 0.037 + 0.032 + 0.056 + 0.059) \approx 6.9mA$$

Power-down Supply Current

Figure 150. Power-down Supply Current vs. V_{CC} (Watchdog Timer Disabled)

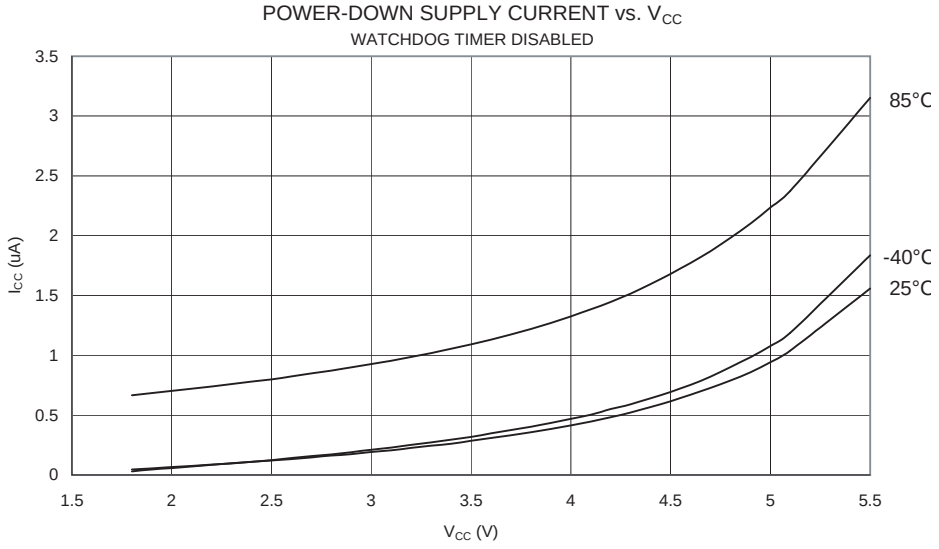
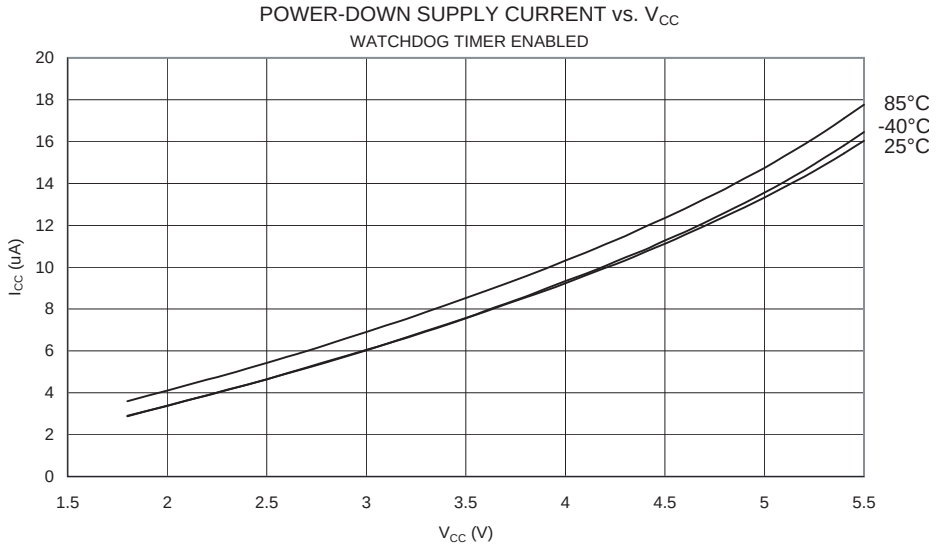
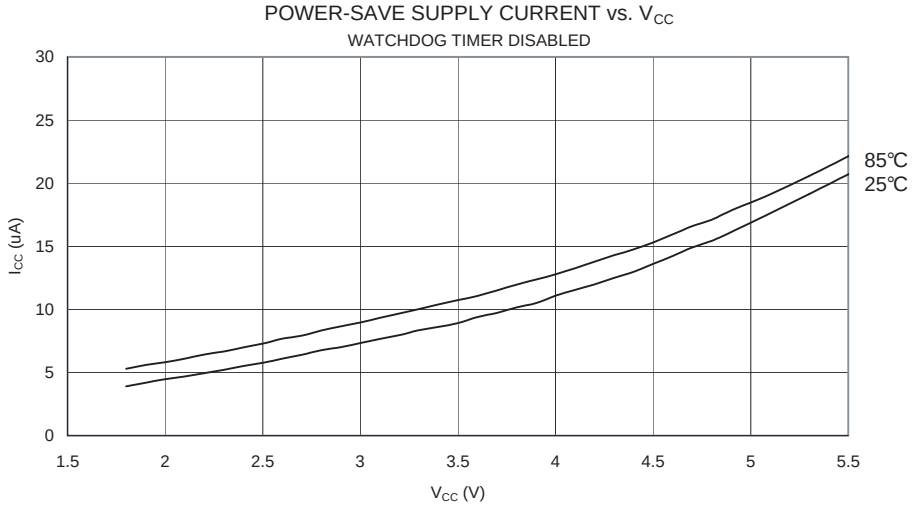


Figure 151. Power-down Supply Current vs. V_{CC} (Watchdog Timer Enabled)



Power-save Supply Current

Figure 152. Power-save Supply Current vs. V_{CC} (Watchdog Timer Disabled)



The differential current consumption between Power-save with WD disabled and 32 kHz TOSC represents the current drawn by Timer/Counter2.

Standby Supply Current

Figure 153. Standby Supply Current vs. V_{CC} (455 kHz Resonator, Watchdog Timer Disabled)

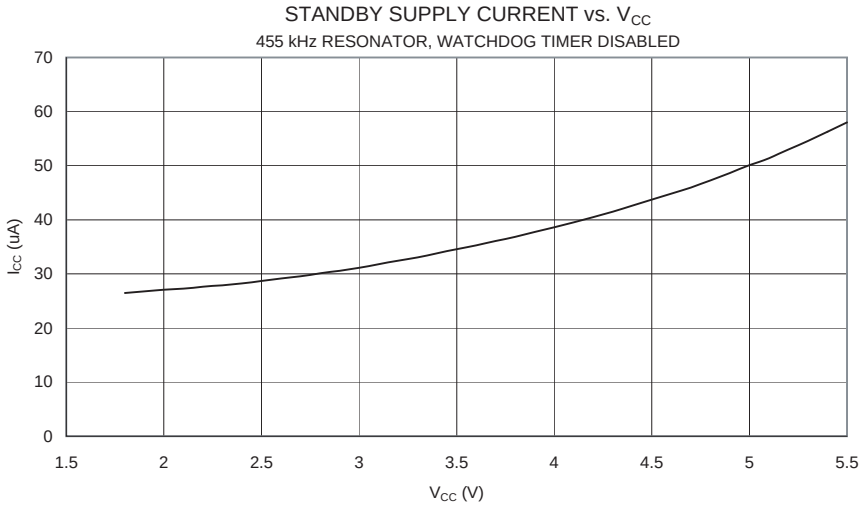


Figure 154. Standby Supply Current vs. V_{CC} (1 MHz Resonator, Watchdog Timer Disabled)

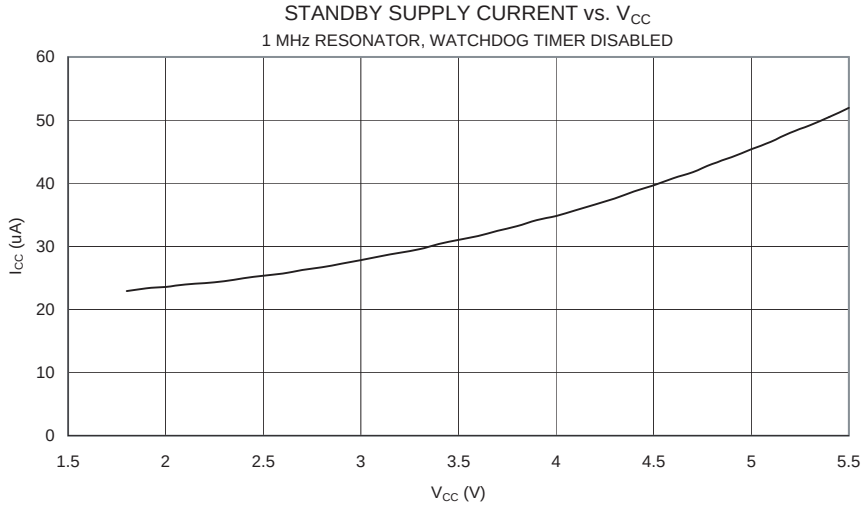


Figure 155. Standby Supply Current vs. V_{CC} (2 MHz Resonator, Watchdog Timer Disabled)

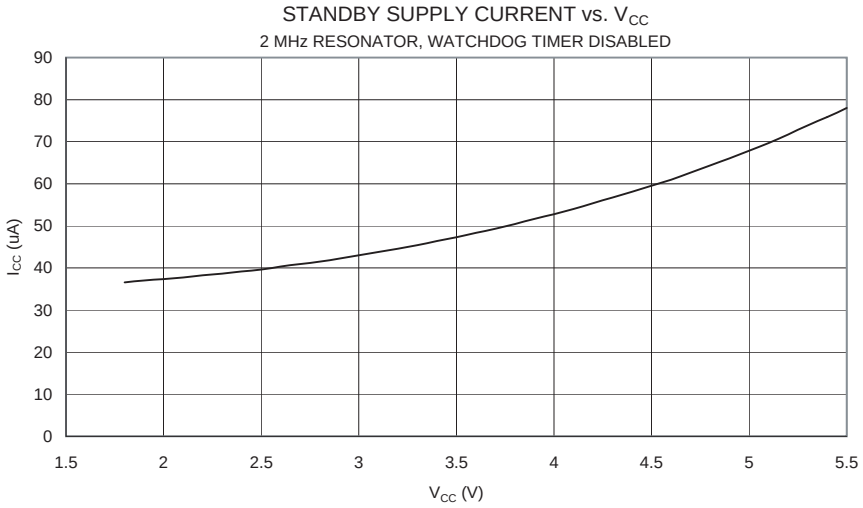


Figure 156. Standby Supply Current vs. V_{CC} (2 MHz Xtal, Watchdog Timer Disabled)

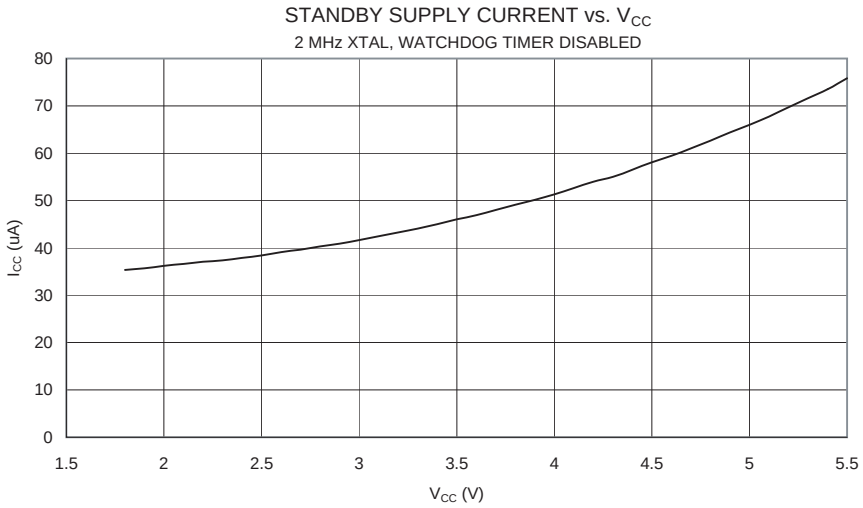


Figure 157. Standby Supply Current vs. V_{CC} (4 MHz Resonator, Watchdog Timer Disabled)

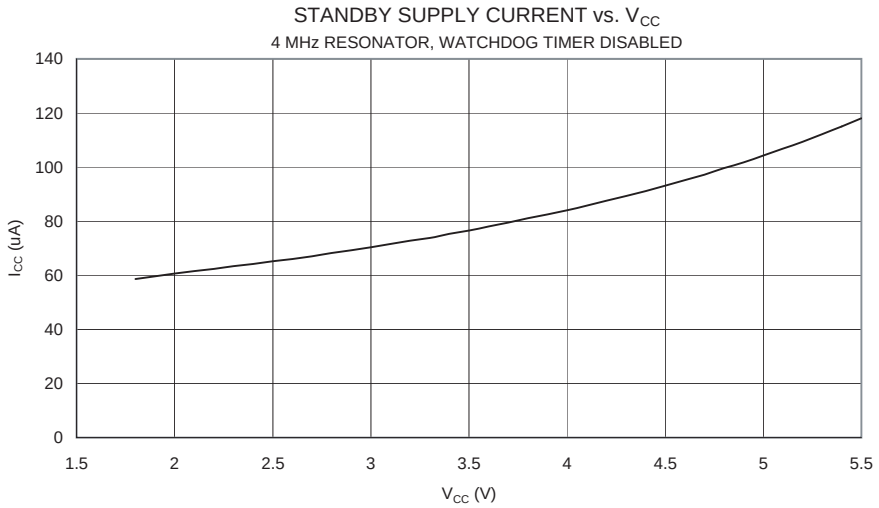


Figure 158. Standby Supply Current vs. V_{CC} (4 MHz Xtal, Watchdog Timer Disabled)

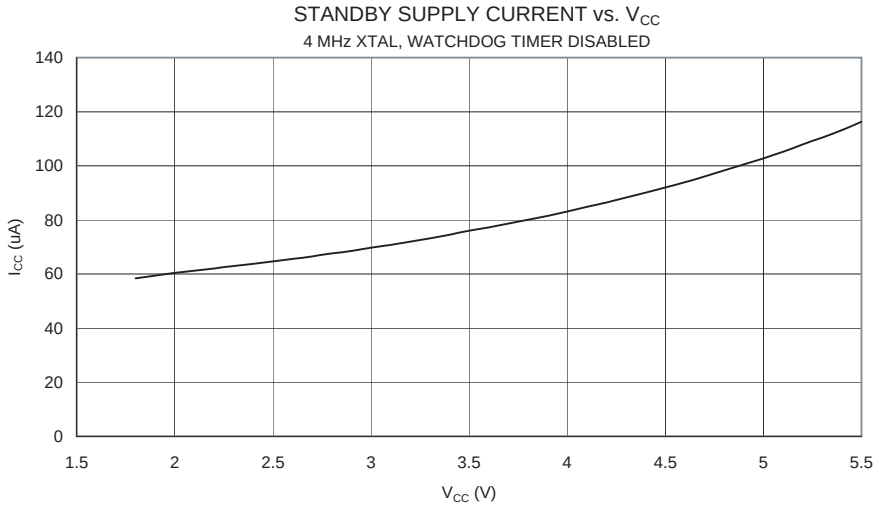


Figure 159. Standby Supply Current vs. V_{CC} (6 MHz Resonator, Watchdog Timer Disabled)

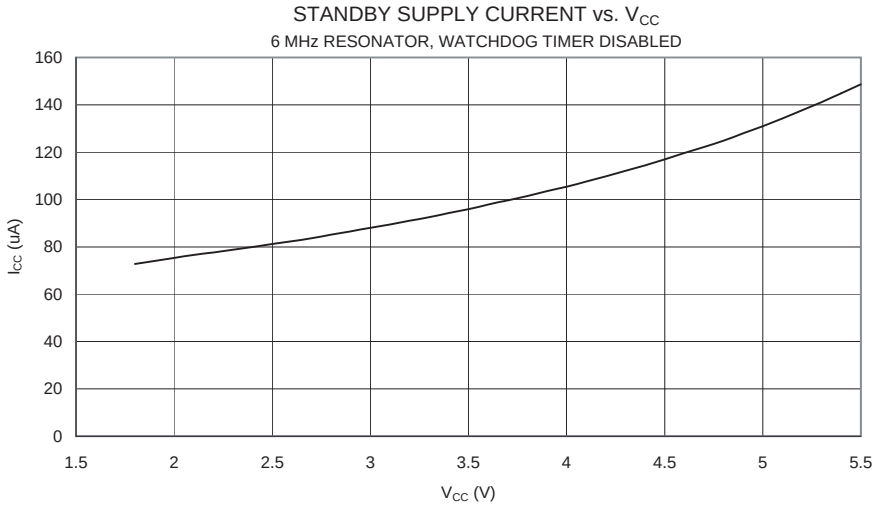
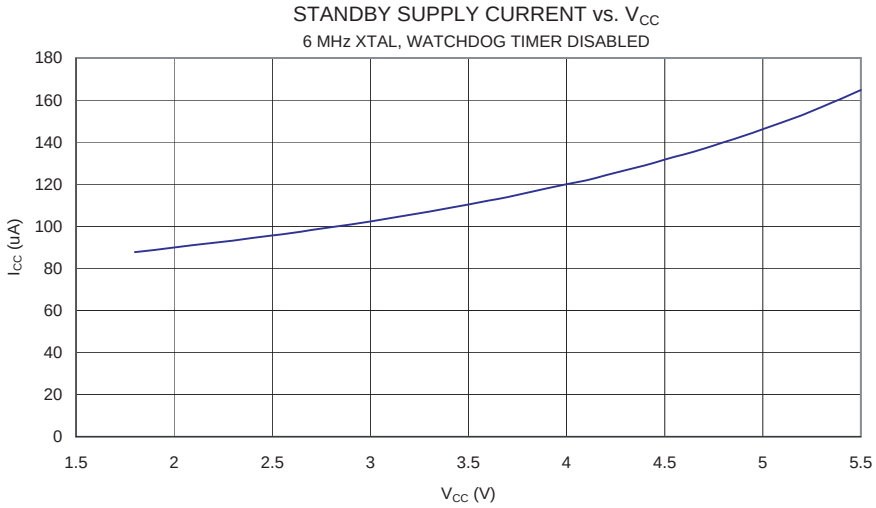


Figure 160. Standby Supply Current vs. V_{CC} (6 MHz Xtal, Watchdog Timer Disabled)



Pin Pull-up

Figure 161. I/O Pin Pull-up Resistor Current vs. Input Voltage (V_{CC} = 5V)

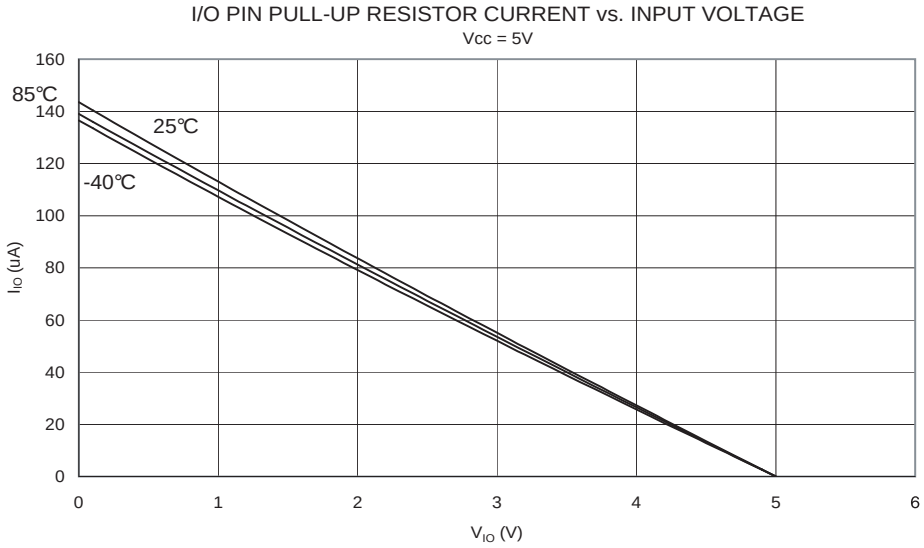


Figure 162. I/O Pin Pull-up Resistor Current vs. Input Voltage (V_{CC} = 2.7V)

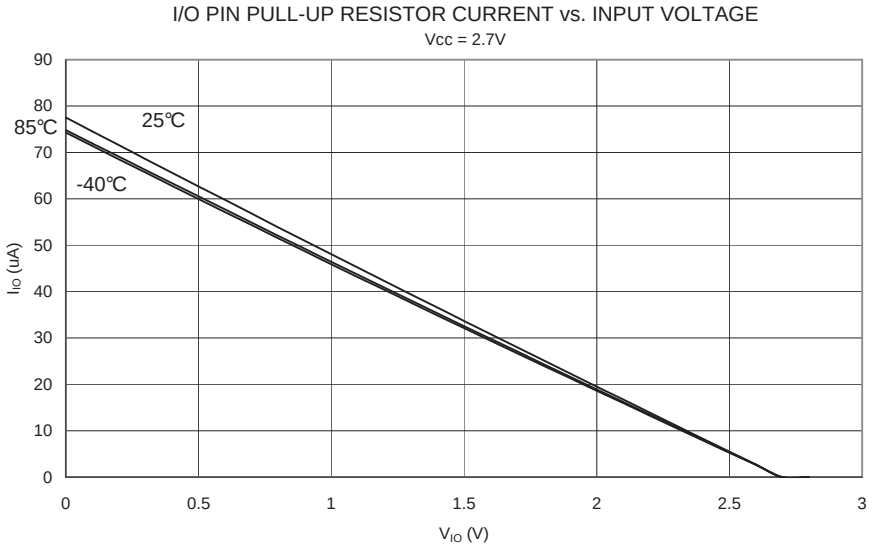


Figure 163. I/O Pin Pull-up Resistor Current vs. Input Voltage (V_{CC} = 1.8V)

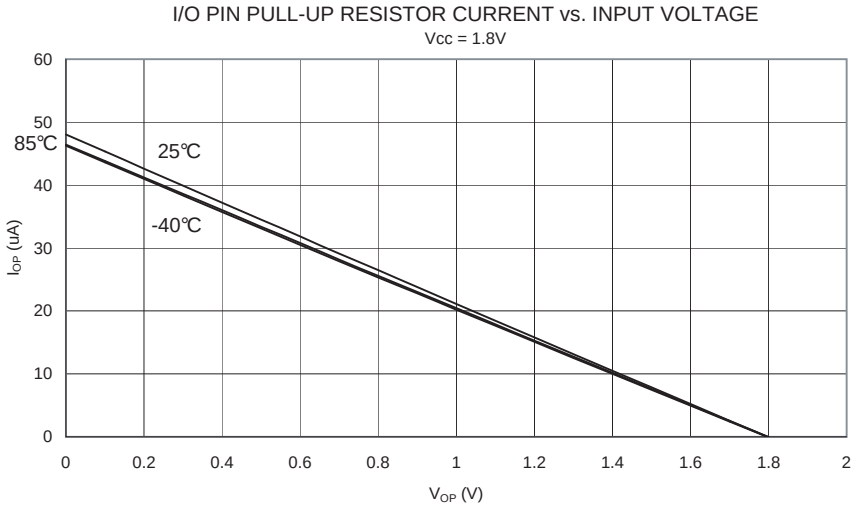


Figure 164. Reset Pull-up Resistor Current vs. Reset Pin Voltage (V_{CC} = 5V)

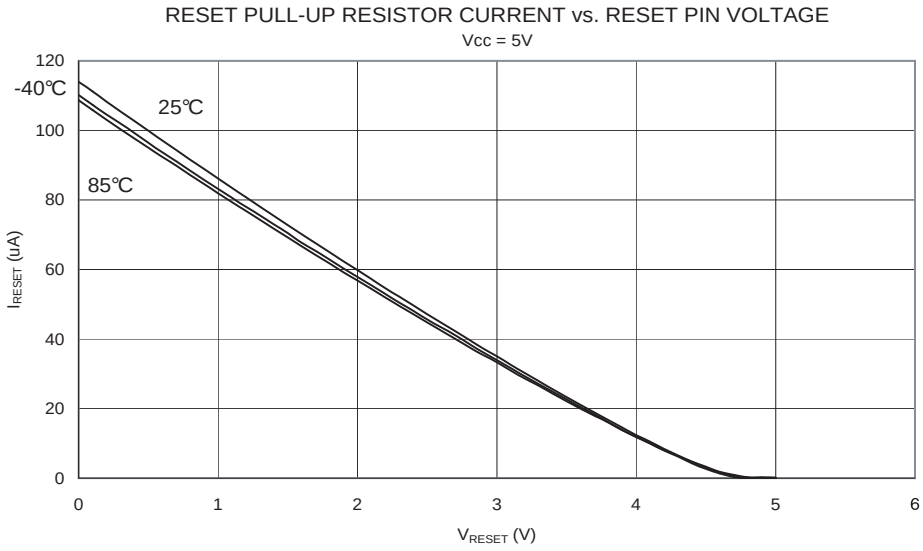


Figure 165. Reset Pull-up Resistor Current vs. Reset Pin Voltage (V_{CC} = 2.7V)

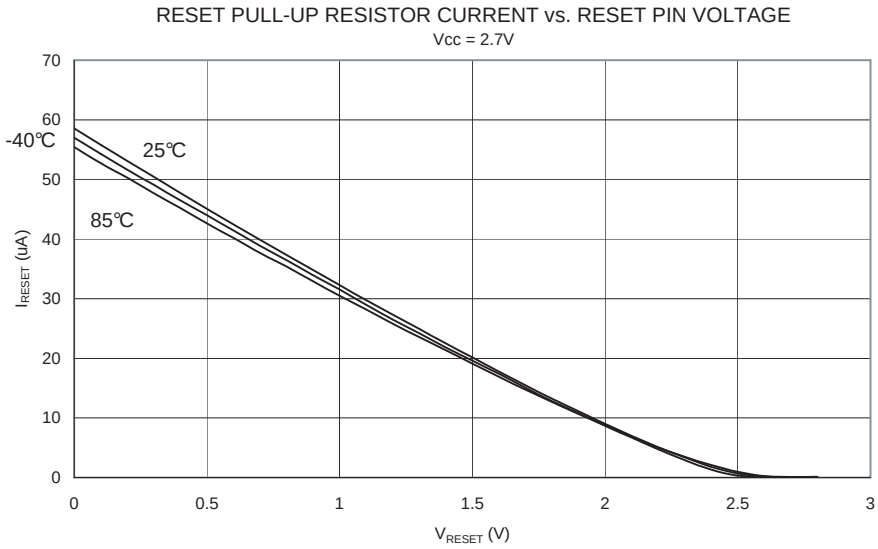
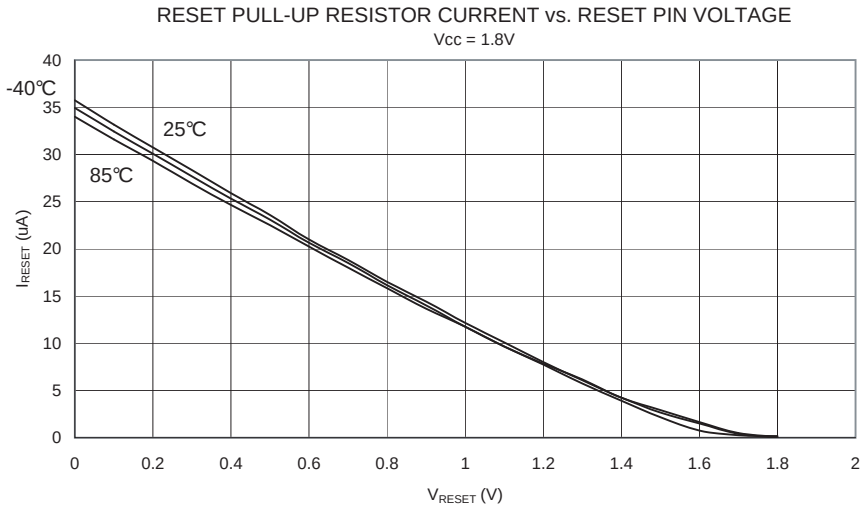


Figure 166. Reset Pull-up Resistor Current vs. Reset Pin Voltage (V_{CC} = 1.8V)



Pin Driver Strength

Figure 167. I/O Pin Source Current vs. Output Voltage, Ports A, C, D, E, F, G (V_{CC} = 5V)

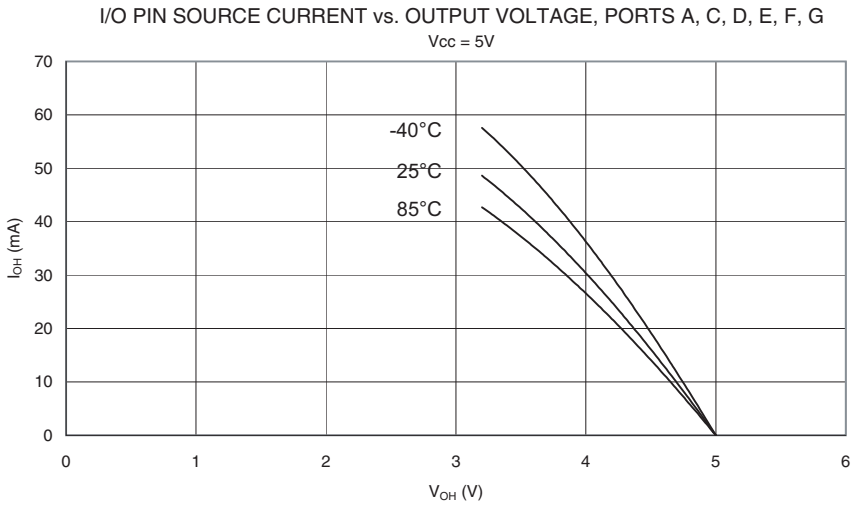


Figure 168. I/O Pin Source Current vs. Output Voltage, Ports A, C, D, E, F, G (V_{CC} = 2.7V)

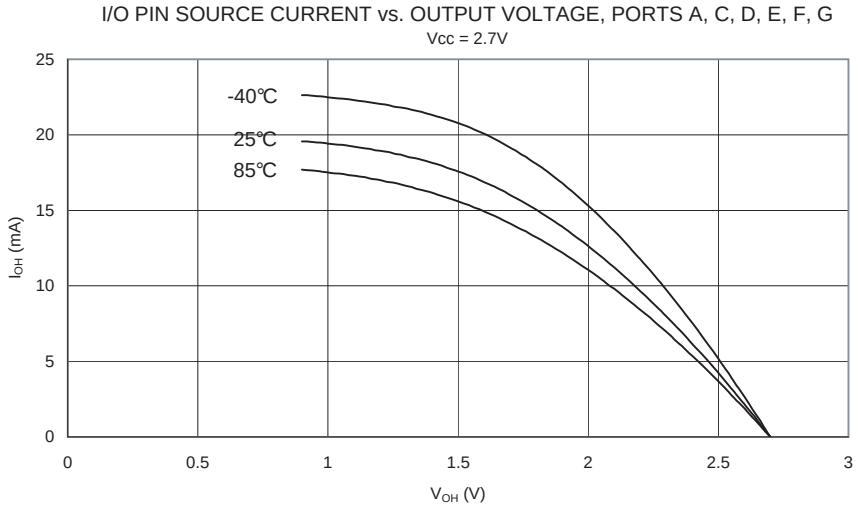


Figure 169. I/O Pin Source Current vs. Output Voltage, Ports A, C, D, E, F, G (V_{CC} = 1.8V)

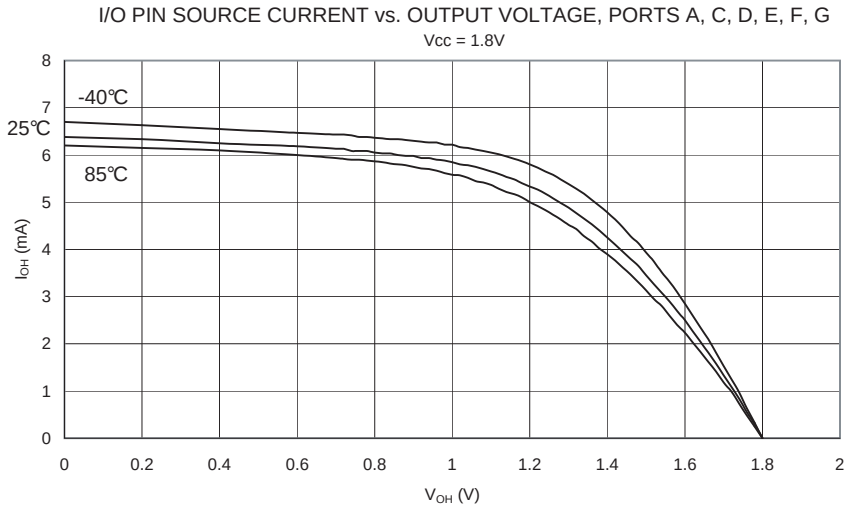


Figure 170. I/O Pin Source Current vs. Output Voltage, Port B (V_{CC}= 5V)

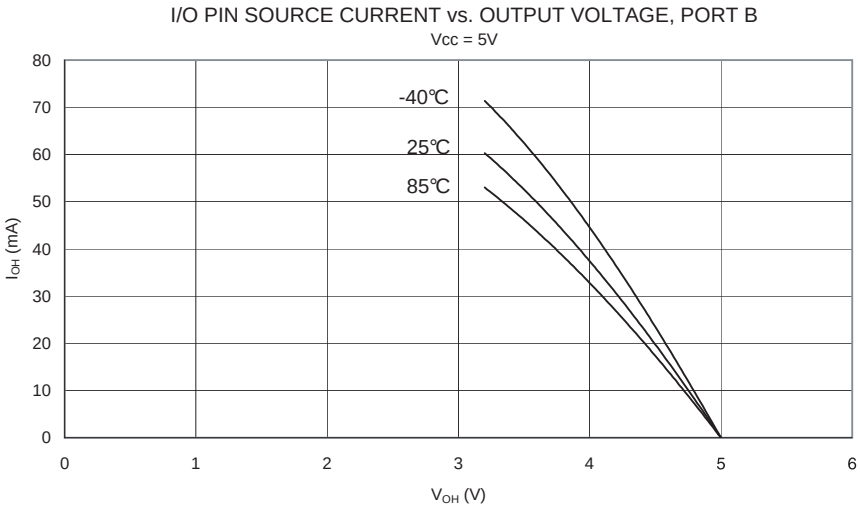


Figure 171. I/O Pin Source Current vs. Output Voltage, Port B (V_{CC} = 2.7V)

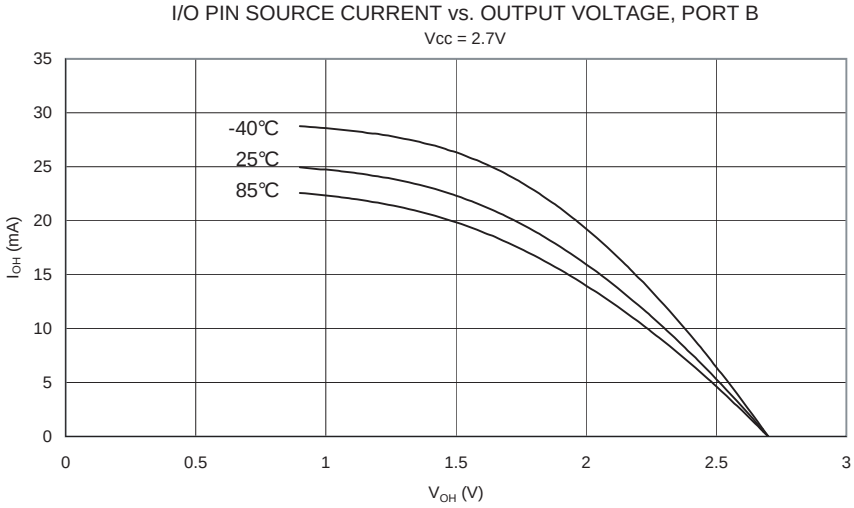


Figure 172. I/O Pin Source Current vs. Output Voltage, Port B (V_{CC} = 1.8V)

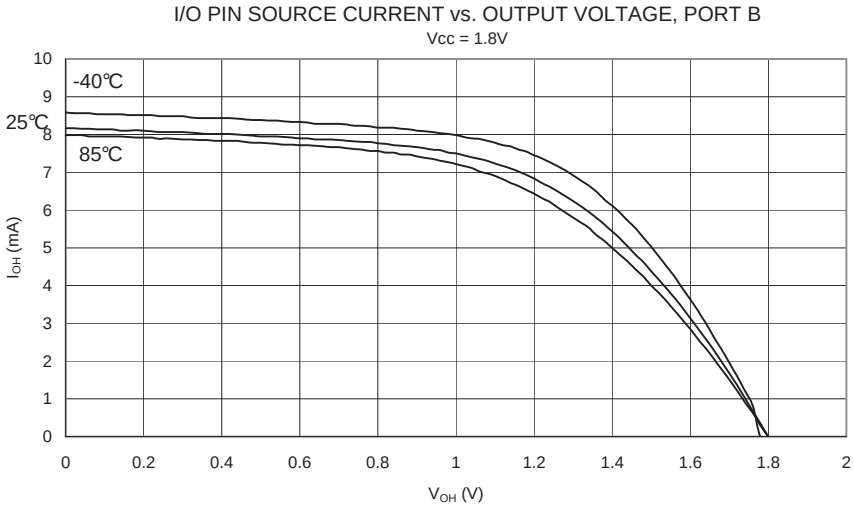


Figure 173. I/O Pin Sink Current vs. Output Voltage, Ports A, C, D, E, F, G (V_{CC} = 5V)

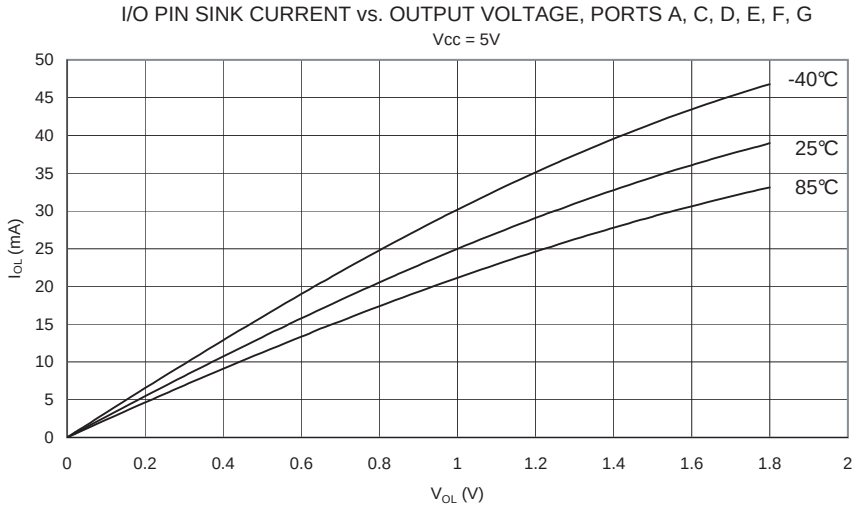


Figure 174. I/O Pin Sink Current vs. Output Voltage, Ports A, C, D, E, F, G (V_{CC} = 2.7V)

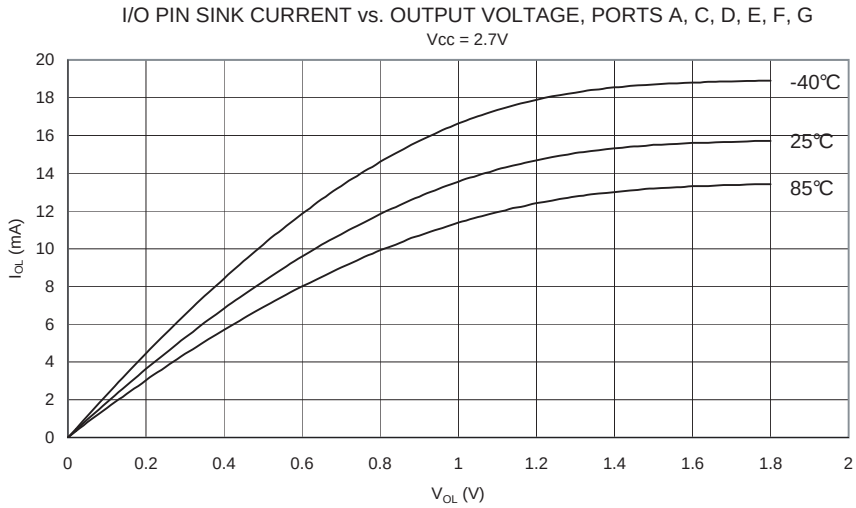


Figure 175. I/O Pin Sink Current vs. Output Voltage, Ports A, C, D, E, F, G (V_{CC} = 1.8V)

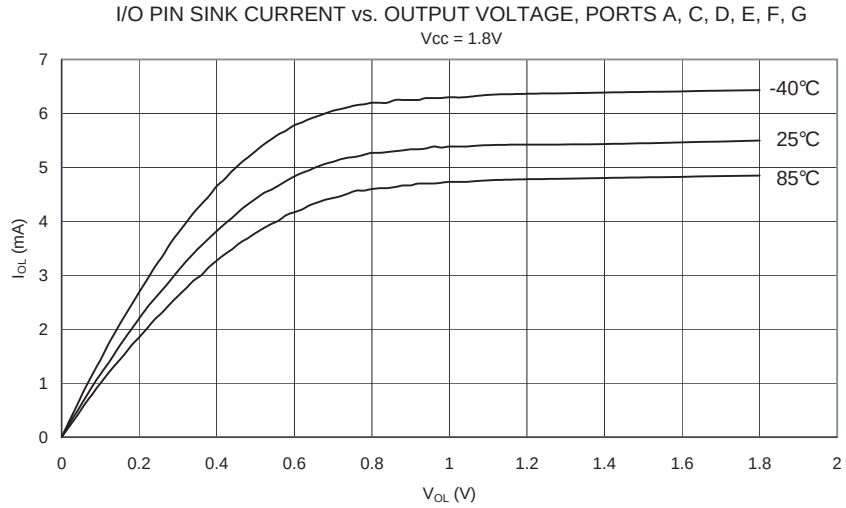


Figure 176. I/O Pin Sink Current vs. Output Voltage, Port B (V_{CC} = 5V)

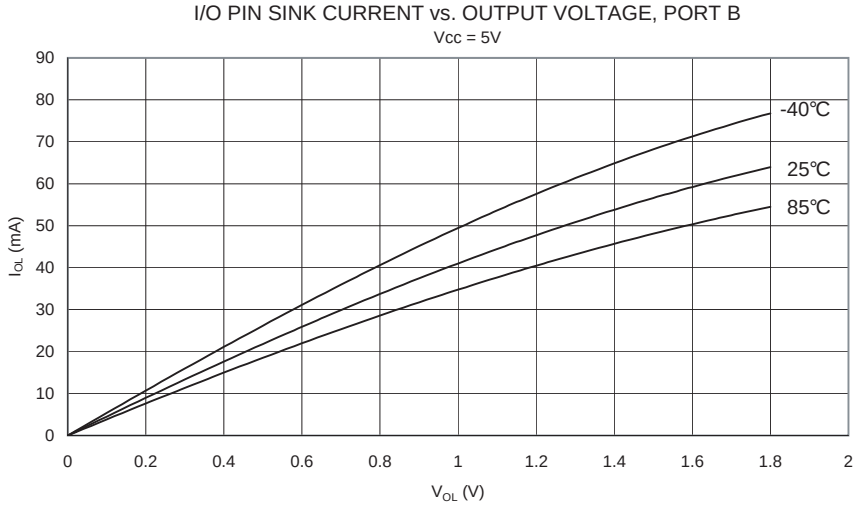


Figure 177. I/O Pin Sink Current vs. Output Voltage, Port B (V_{CC} = 2.7V)

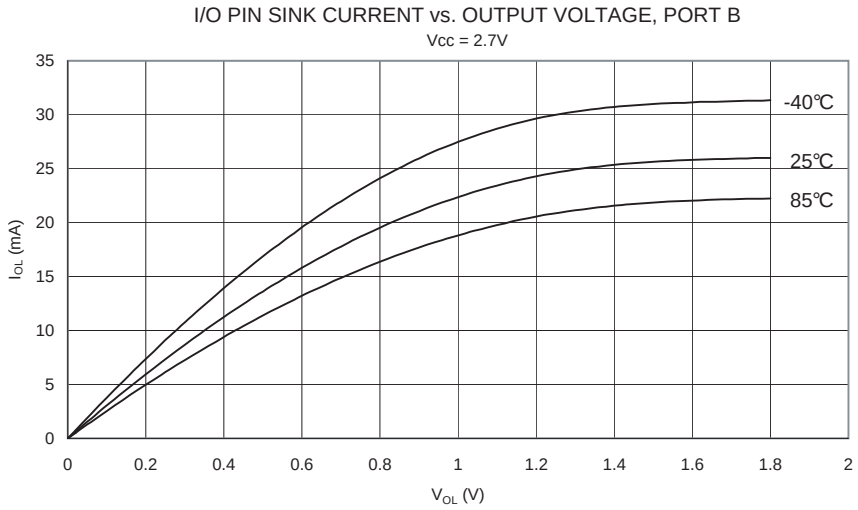
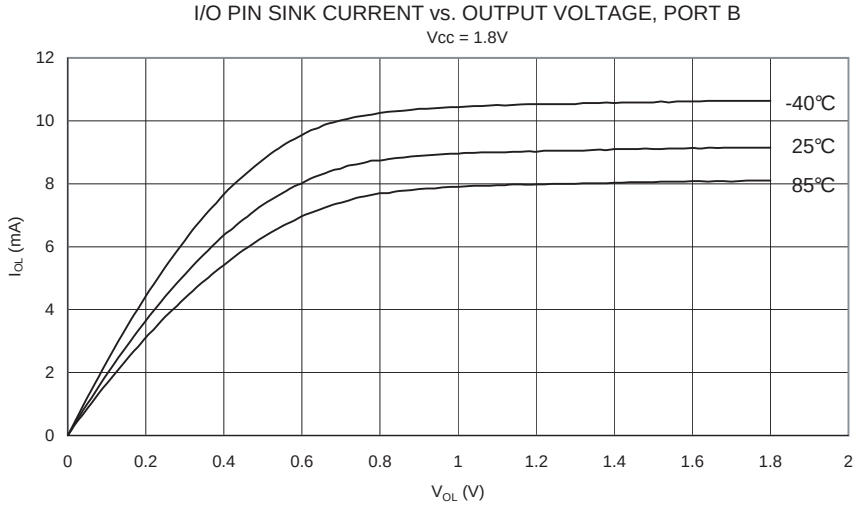


Figure 178. I/O Pin Sink Current vs. Output Voltage, Port B (V_{CC} = 1.8V)



Pin Thresholds and hysteresis

Figure 179. I/O Pin Input Threshold Voltage vs. V_{CC} (V_{IH}, I/O Pin Read as “1”)

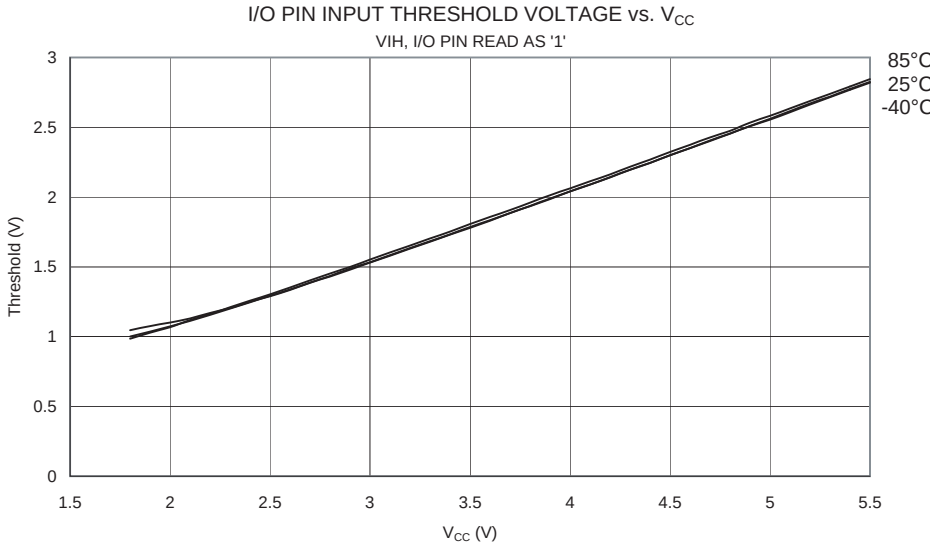


Figure 180. I/O Pin Input Threshold Voltage vs. V_{CC} (V_{IL}, I/O Pin Read as “0”)

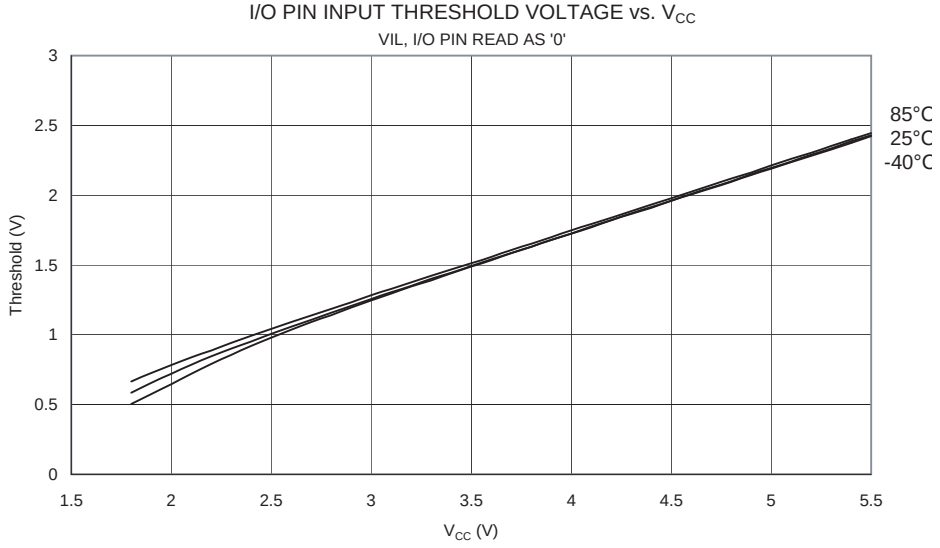


Figure 181. I/O Pin Input Hysteresis vs. V_{CC}

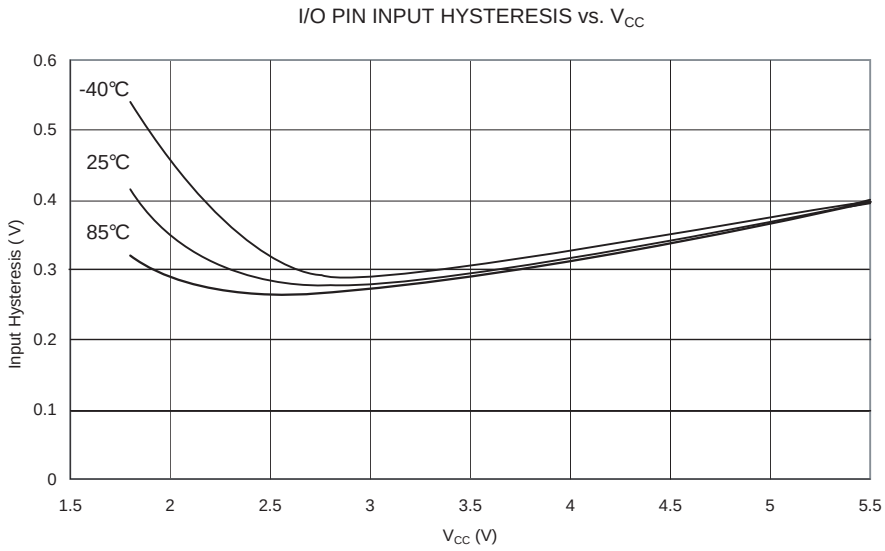


Figure 182. Reset Input Threshold Voltage vs. V_{CC} (V_{IH},Reset Pin Read as “1”)

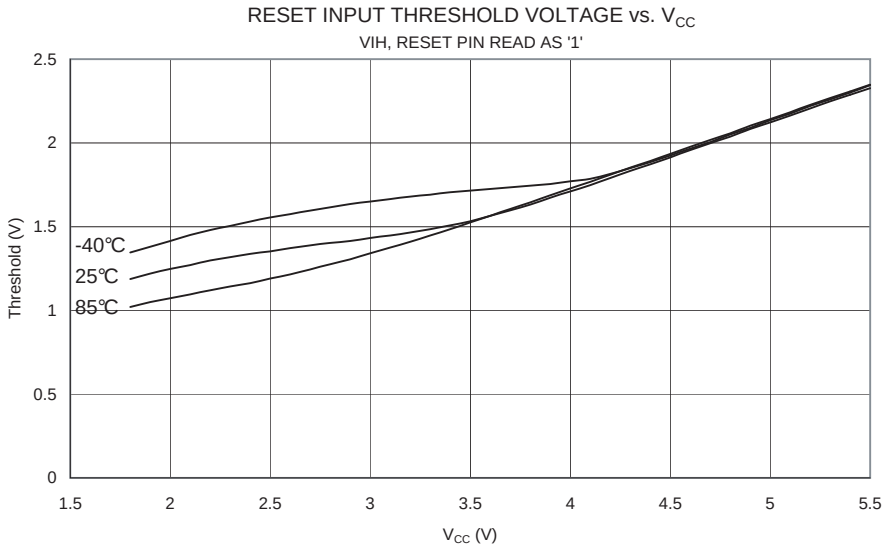


Figure 183. Reset Input Threshold Voltage vs. V_{CC} (V_{IL},Reset Pin Read as “0”)

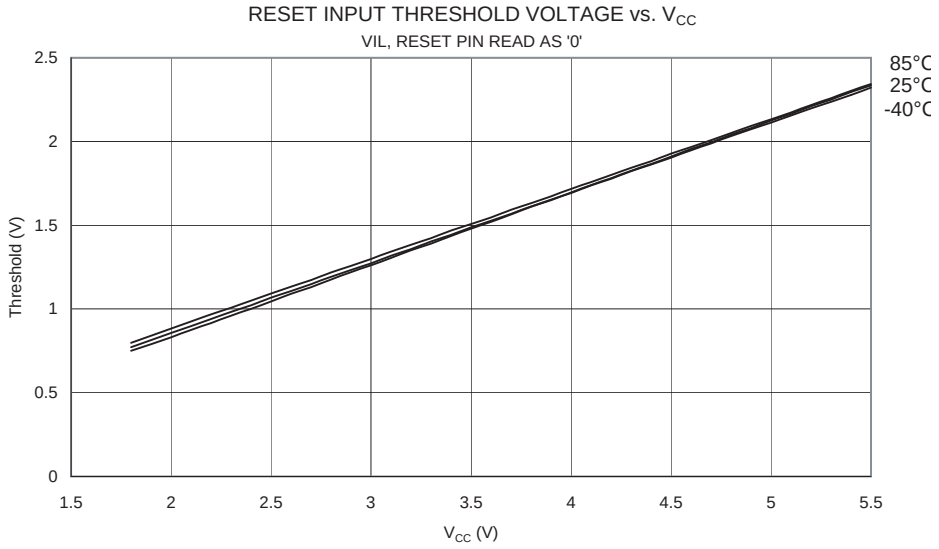
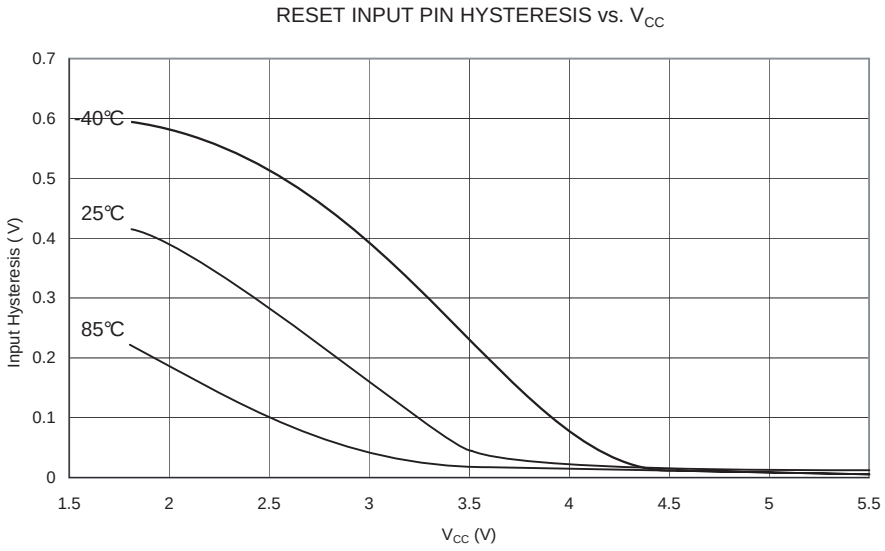


Figure 184. Reset Input Pin Hysteresis vs. V_{CC}



BOD Thresholds and Analog Comparator Offset

Figure 185. BOD Thresholds vs. Temperature (BOD Level is 4.3V)

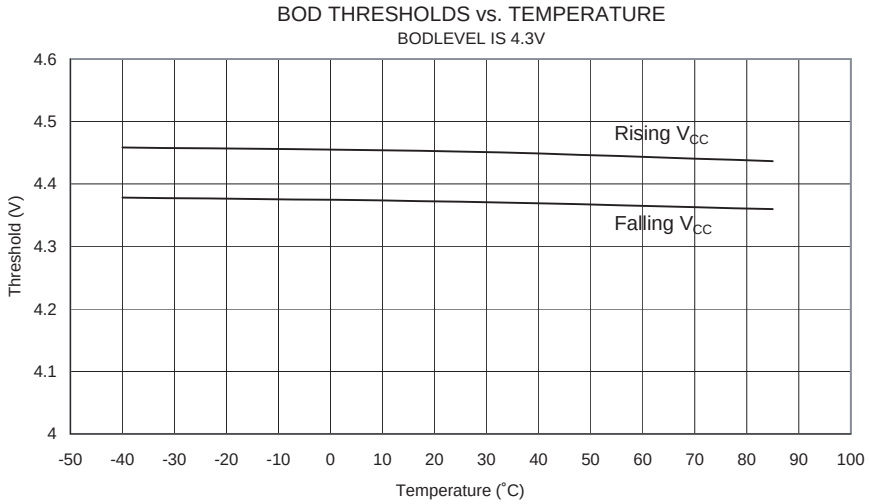


Figure 186. BOD Thresholds vs. Temperature (BOD Level is 2.7V)

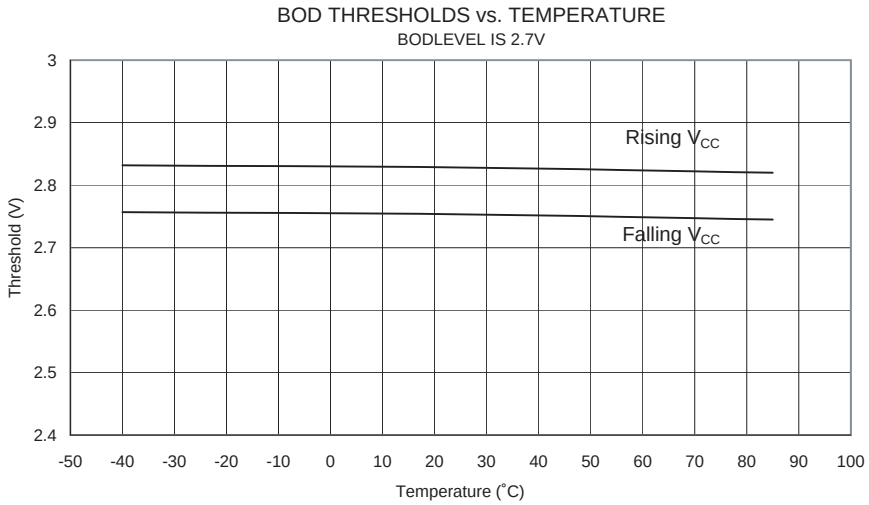


Figure 187. BOD Thresholds vs. Temperature (BOD Level is 1.8V)

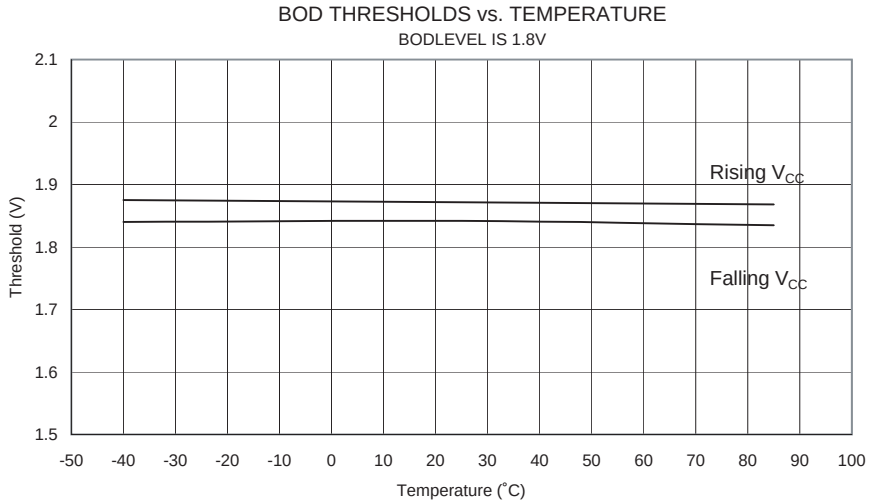


Figure 188. Bandgap Voltage vs. V_{CC}

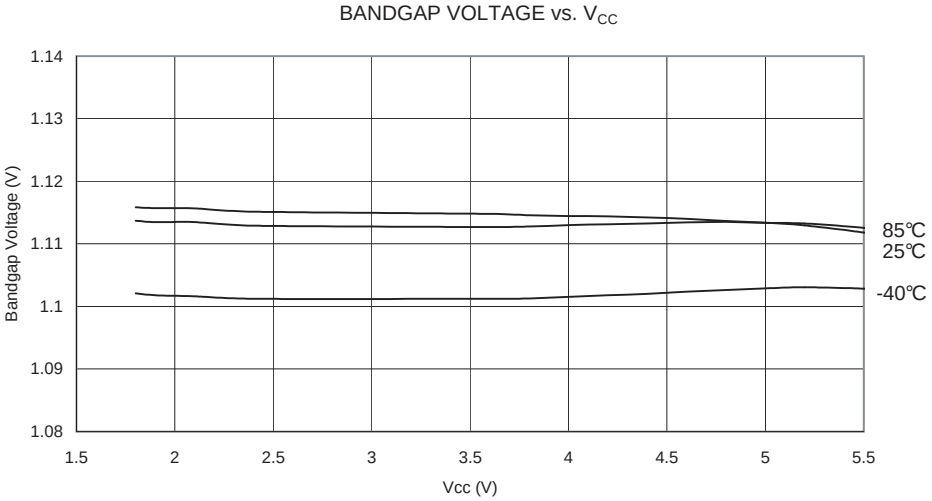


Figure 189. Analog Comparator Offset Voltage vs. Common Mode Voltage (V_{CC} = 5V)

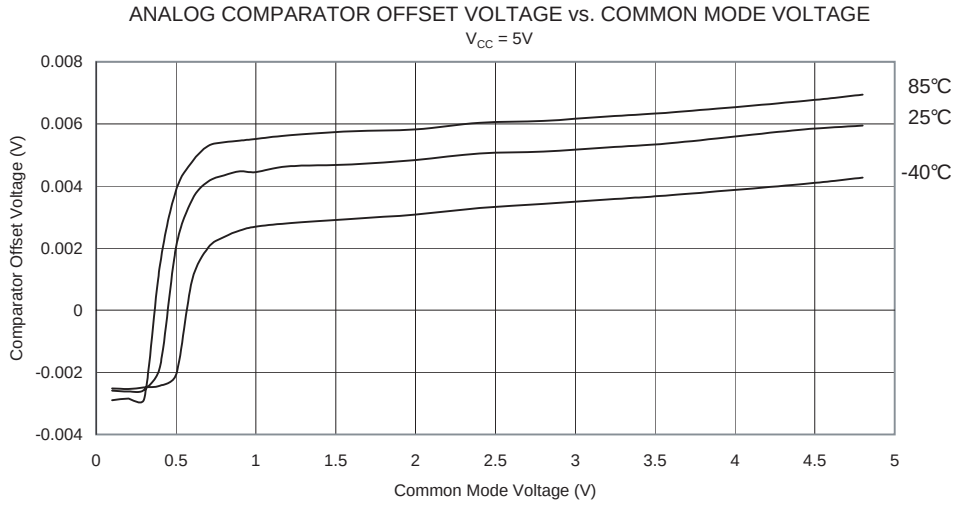
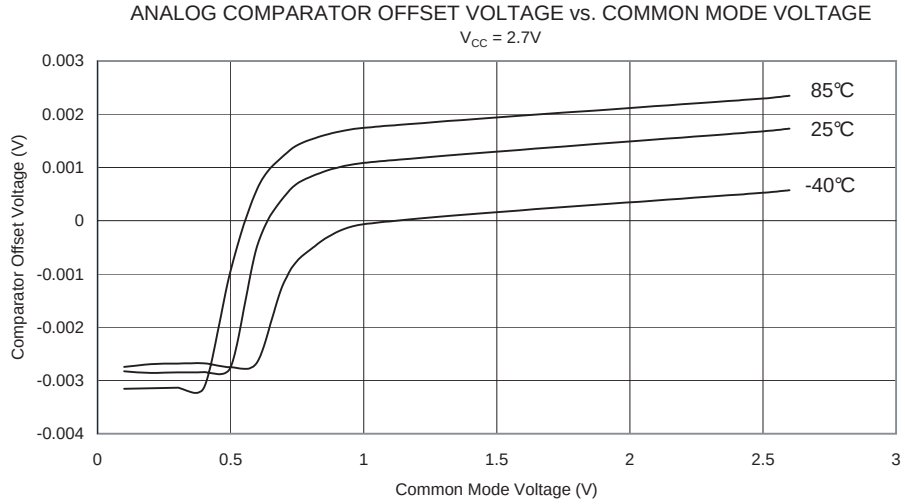


Figure 190. Analog Comparator Offset Voltage vs. Common Mode Voltage (V_{CC} = 2.7V)



Internal Oscillator Speed

Figure 191. Watchdog Oscillator Frequency vs. V_{CC}

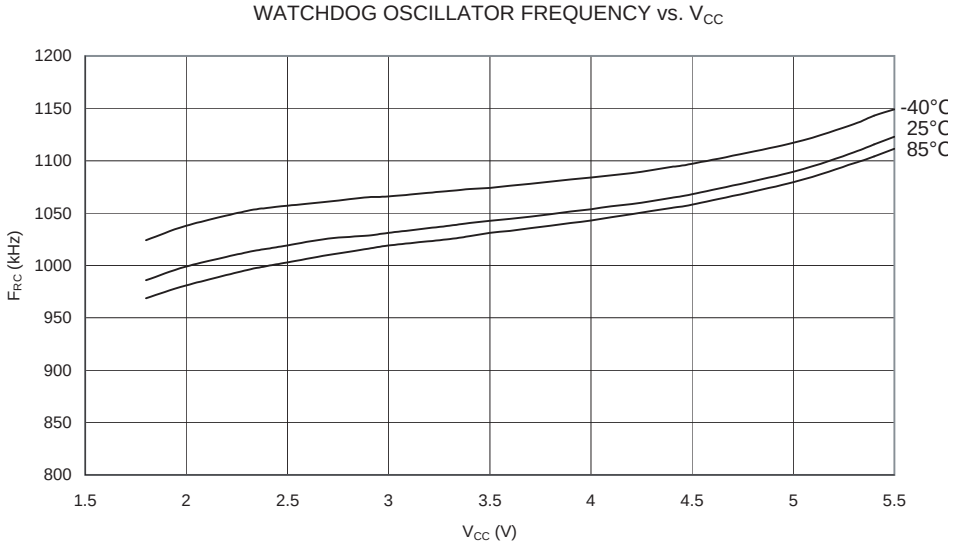


Figure 192. Calibrated 8 MHz RC Oscillator Frequency vs. Temperature

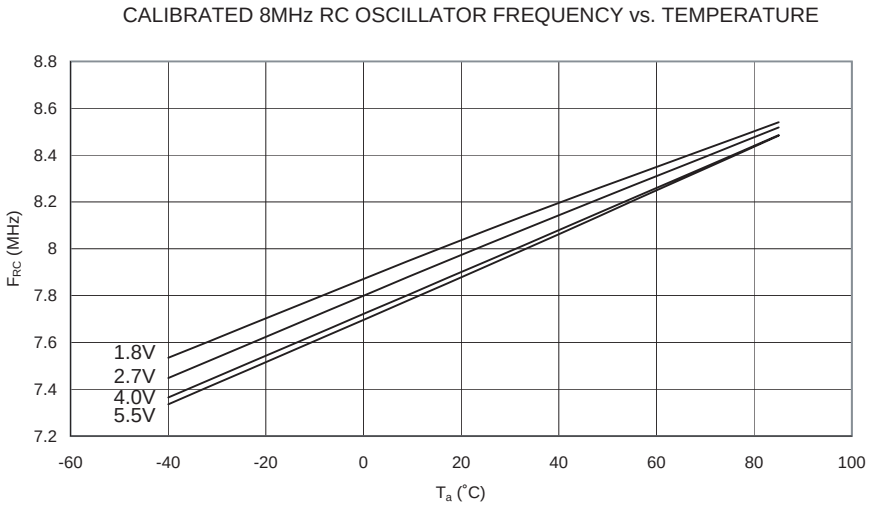


Figure 193. Calibrated 8 MHz RC Oscillator Frequency vs. V_{CC}

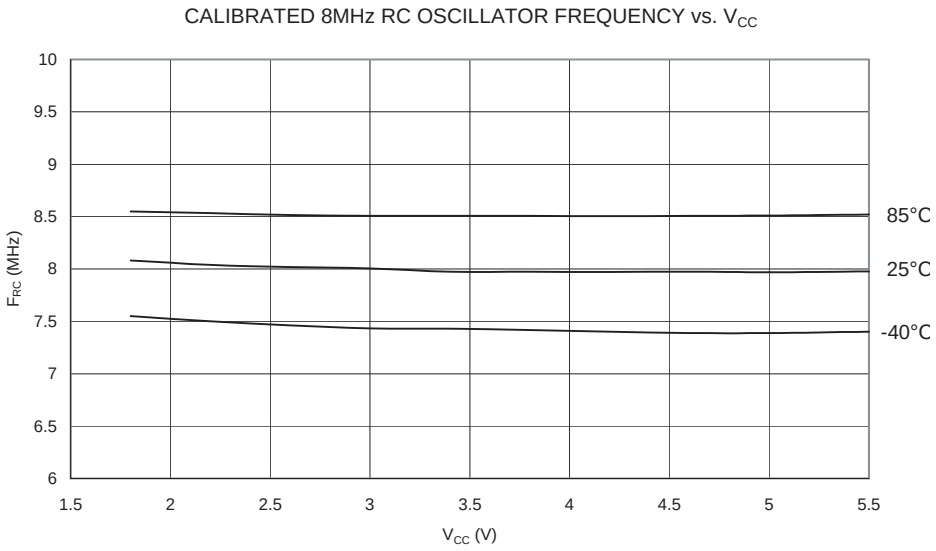
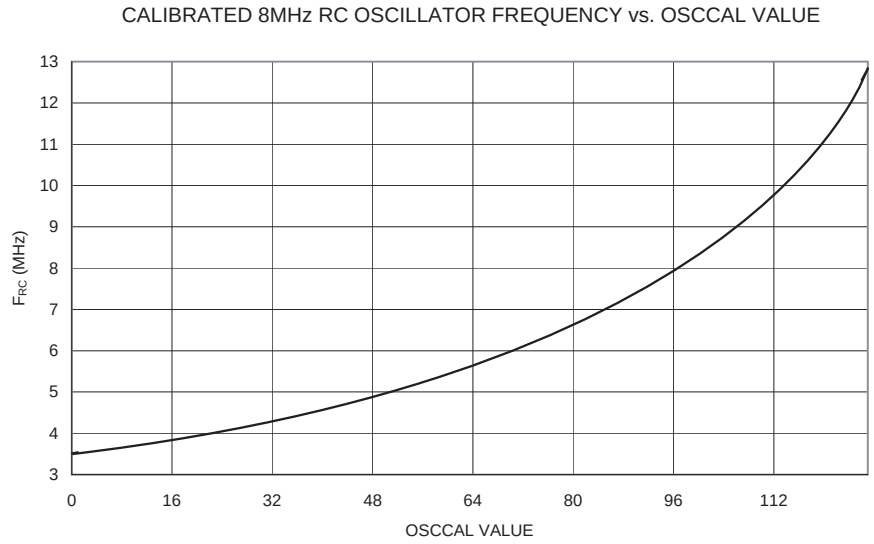


Figure 194. Calibrated 8 MHz RC Oscillator Frequency vs. Osccal Value



Current Consumption of Peripheral Units

Figure 195. Brownout Detector Current vs. V_{CC}

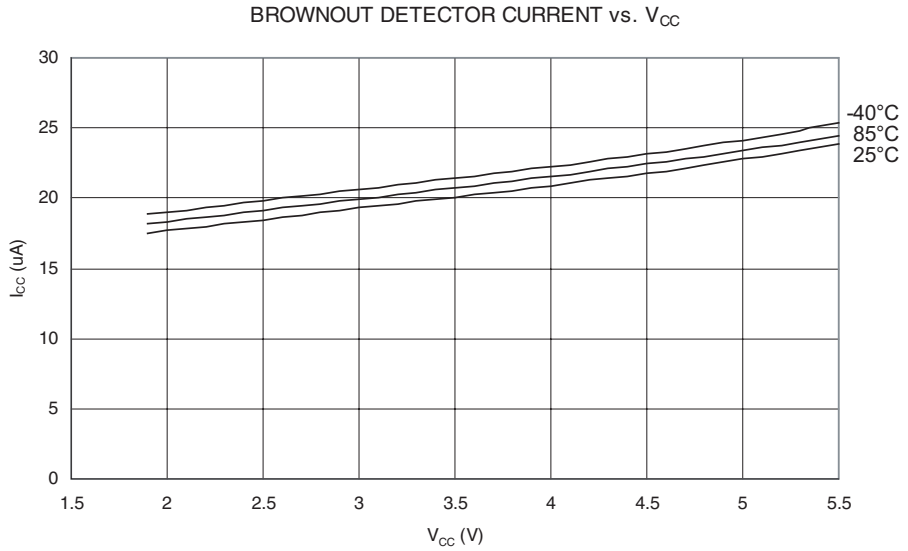


Figure 196. ADC Current vs. V_{CC} (AREF = AVCC)

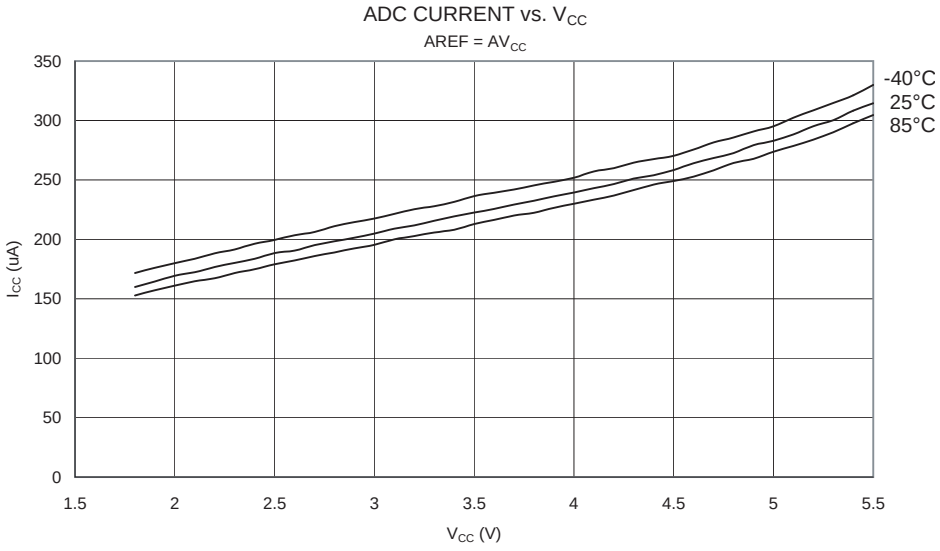


Figure 197. AREF External Reference Current vs. V_{CC}

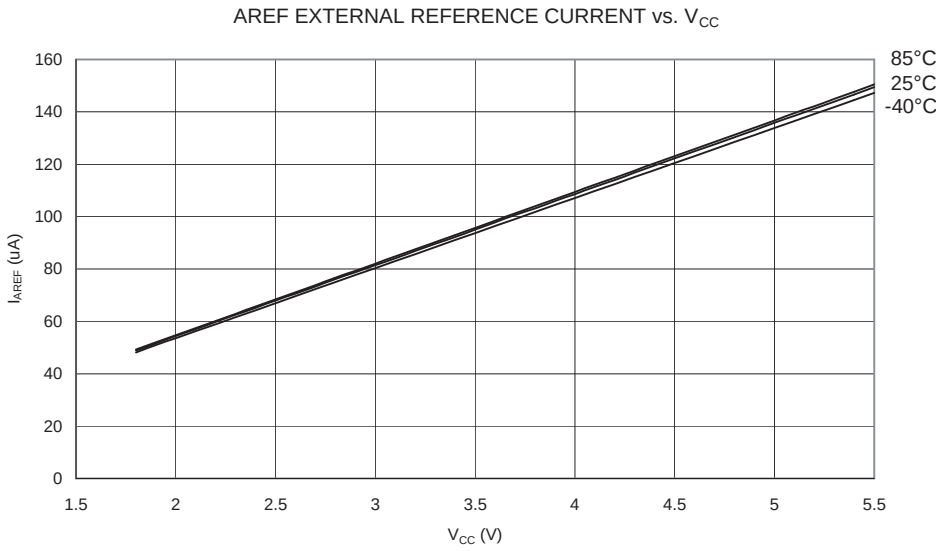
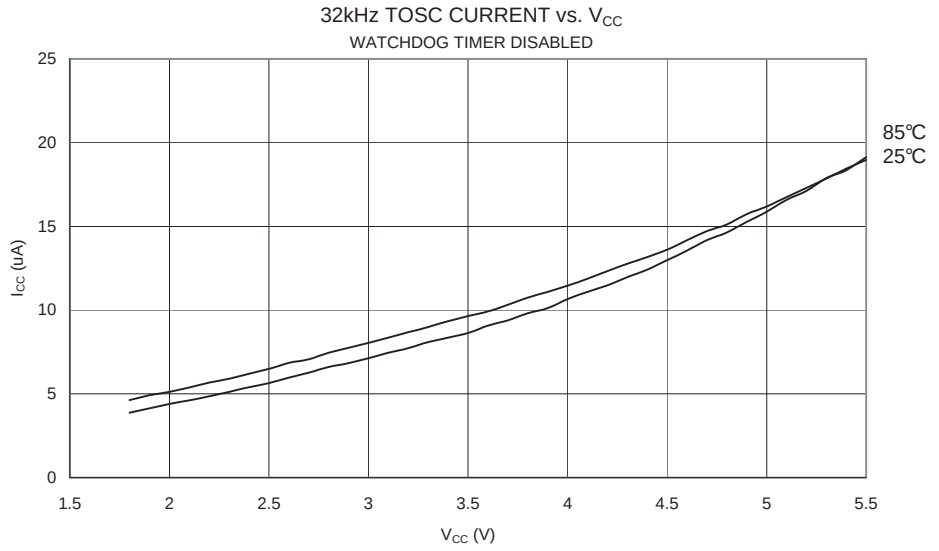


Figure 198. 32 kHZ TOSC Current vs. V_{CC} (Watchdog Timer Disabled)



The differential current consumption between Power-save with WD disabled and 32 kHz TOSC represents the current drawn by Timer/Counter2.

Figure 199. Watchdog Timer Current vs. V_{CC}

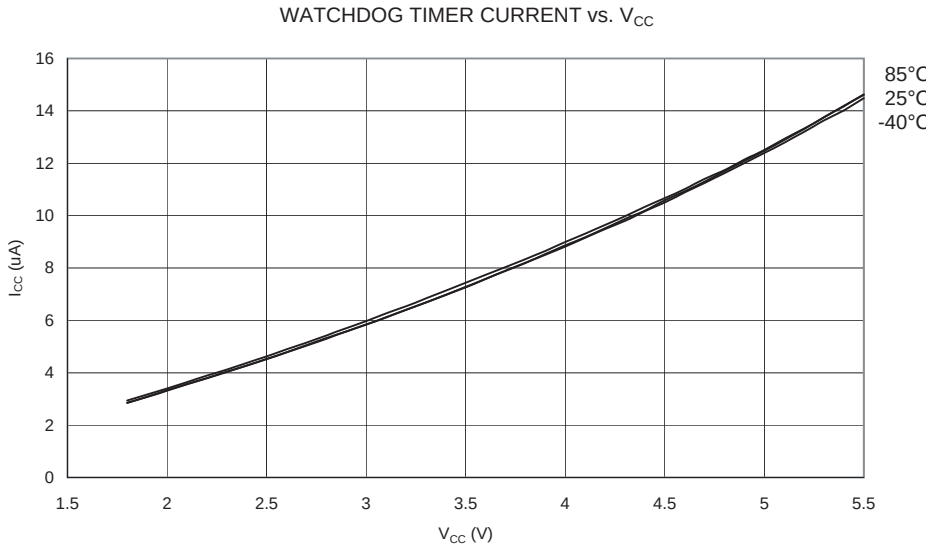


Figure 200. Analog Comparator Current vs. V_{CC}

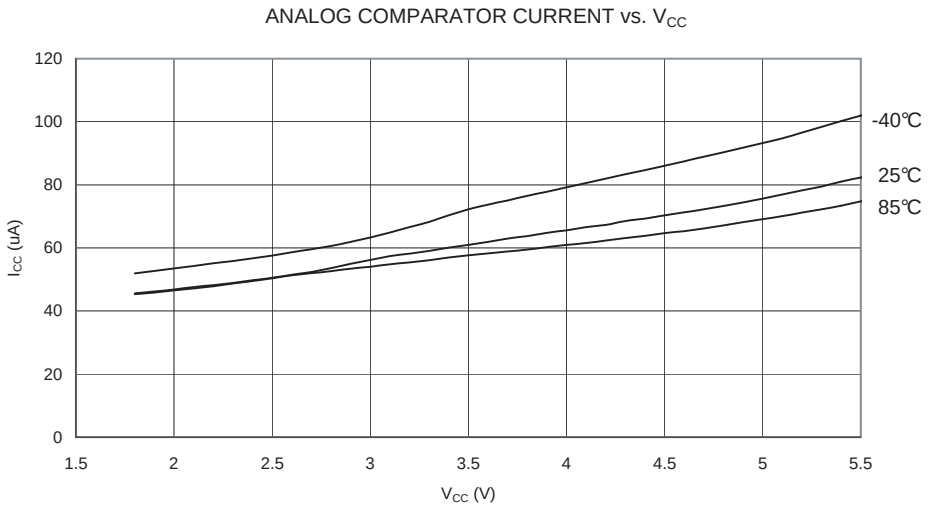
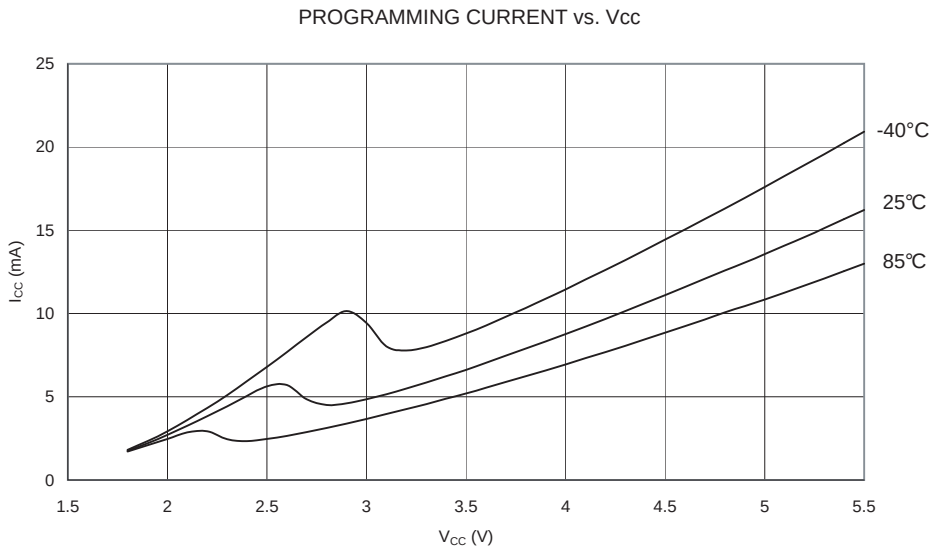


Figure 201. Programming Current vs. V_{CC}



Current Consumption in Reset and Reset Pulsewidth

Figure 202. Reset Supply Current vs. V_{CC} (0.1 - 1.0 MHz, Excluding Current Through The Reset Pull-up)

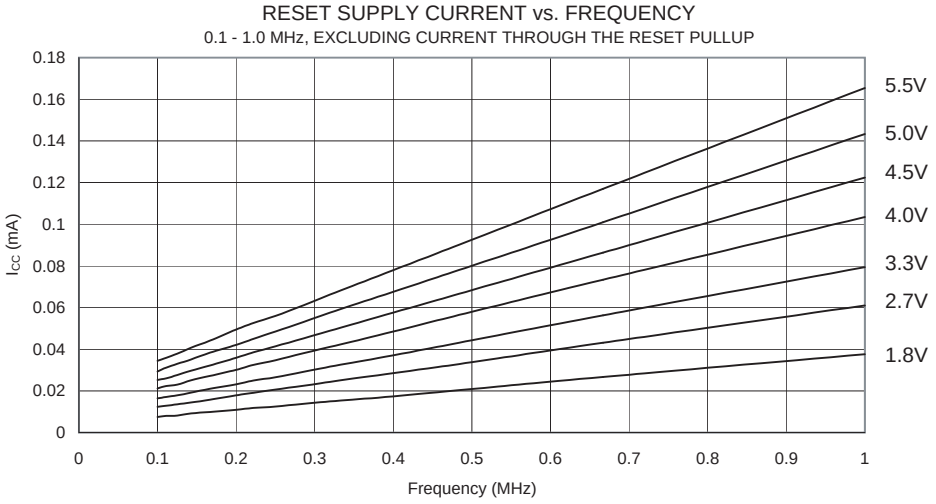


Figure 203. Reset Supply Current vs. V_{CC} (1 - 20 MHz, Excluding Current Through The Reset Pull-up)

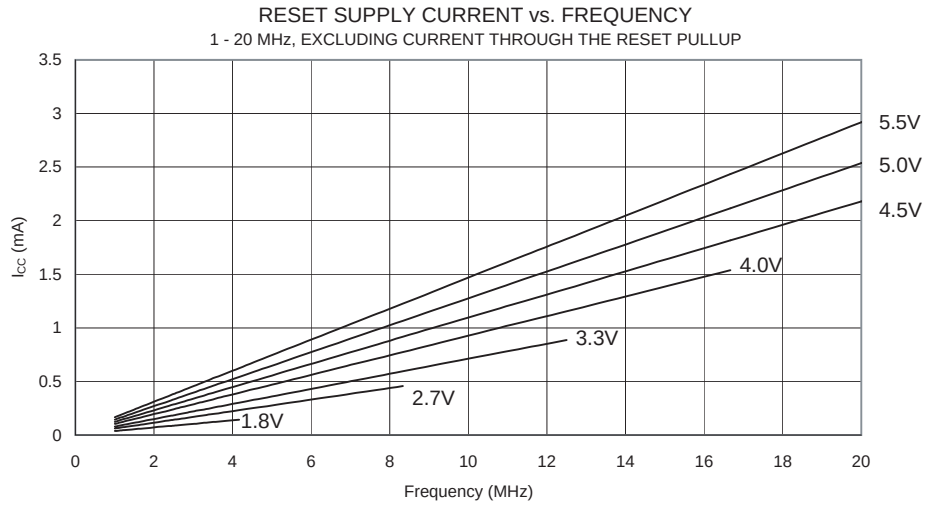
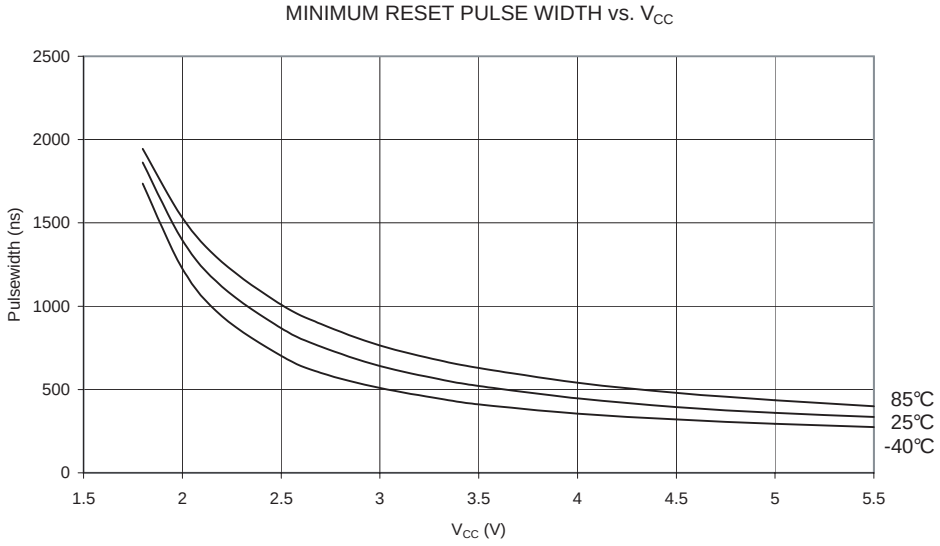


Figure 204. Minimum Reset Pulse Width vs. V_{CC}



Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xFF)	Reserved	–	–	–	–	–	–	–	–	
(0xFE)	LCDDR18	–	–	–	–	–	–	–	SEG324	225
(0xFD)	LCDDR17	SEG323	SEG322	SEG321	SEG320	SEG319	SEG318	SEG317	SEG316	225
(0xFC)	LCDDR16	SEG315	SEG314	SEG313	SEG312	SEG311	SEG310	SEG309	SEG308	225
(0xFB)	LCDDR15	SEG307	SEG306	SEG305	SEG304	SEG303	SEG302	SEG301	SEG300	225
(0xFA)	Reserved	–	–	–	–	–	–	–	–	
(0xF9)	LCDDR13	–	–	–	–	–	–	–	SEG224	225
(0xF8)	LCDDR12	SEG223	SEG222	SEG221	SEG220	SEG219	SEG218	SEG217	SEG216	225
(0xF7)	LCDDR11	SEG215	SEG214	SEG213	SEG212	SEG211	SEG210	SEG209	SEG208	225
(0xF6)	LCDDR10	SEG207	SEG206	SEG205	SEG204	SEG203	SEG202	SEG201	SEG200	225
(0xF5)	Reserved	–	–	–	–	–	–	–	–	
(0xF4)	LCDDR8	–	–	–	–	–	–	–	SEG124	225
(0xF3)	LCDDR7	SEG123	SEG122	SEG121	SEG120	SEG119	SEG118	SEG117	SEG116	225
(0xF2)	LCDDR6	SEG115	SEG114	SEG113	SEG112	SEG111	SEG110	SEG109	SEG108	225
(0xF1)	LCDDR5	SEG107	SEG106	SEG105	SEG104	SEG103	SEG102	SEG101	SEG100	225
(0xF0)	Reserved	–	–	–	–	–	–	–	–	
(0xEF)	LCDDR3	–	–	–	–	–	–	–	SEG024	225
(0xEE)	LCDDR2	SEG023	SEG022	SEG021	SEG020	SEG019	SEG018	SEG017	SEG016	225
(0xED)	LCDDR1	SEG015	SEG014	SEG013	SEG012	SEG011	SEG010	SEG09	SEG008	225
(0xEC)	LCDDR0	SEG007	SEG006	SEG005	SEG004	SEG003	SEG002	SEG001	SEG000	225
(0xEB)	Reserved	–	–	–	–	–	–	–	–	
(0xEA)	Reserved	–	–	–	–	–	–	–	–	
(0xE9)	Reserved	–	–	–	–	–	–	–	–	
(0xE8)	Reserved	–	–	–	–	–	–	–	–	
(0xE7)	LCDCCR	LCDCD2	LCDCD1	LCDCC0	–	LCDCC3	LCDCC2	LCDCC1	LCDCC0	223
(0xE6)	LCDFRR	–	LCDPS2	LCDPS1	LCDPS0	–	LCDCD2	LCDCD1	LCDCD0	221
(0xE5)	LCDCRB	LCDCS	LCD2B	LCDMUX1	LCDMUX0	–	LCDPM2	LCDPM1	LCDPM0	220
(0xE4)	LCDCRA	LCDEN	LCDAB	–	LCDIF	LCDIE	–	–	LCDBL	219
(0xE3)	Reserved	–	–	–	–	–	–	–	–	
(0xE2)	Reserved	–	–	–	–	–	–	–	–	
(0xE1)	Reserved	–	–	–	–	–	–	–	–	
(0xE0)	Reserved	–	–	–	–	–	–	–	–	
(0xDF)	Reserved	–	–	–	–	–	–	–	–	
(0xDE)	Reserved	–	–	–	–	–	–	–	–	
(0xDD)	Reserved	–	–	–	–	–	–	–	–	
(0xDC)	Reserved	–	–	–	–	–	–	–	–	
(0xDB)	Reserved	–	–	–	–	–	–	–	–	
(0xDA)	Reserved	–	–	–	–	–	–	–	–	
(0xD9)	Reserved	–	–	–	–	–	–	–	–	
(0xD8)	Reserved	–	–	–	–	–	–	–	–	
(0xD7)	Reserved	–	–	–	–	–	–	–	–	
(0xD6)	Reserved	–	–	–	–	–	–	–	–	
(0xD5)	Reserved	–	–	–	–	–	–	–	–	
(0xD4)	Reserved	–	–	–	–	–	–	–	–	
(0xD3)	Reserved	–	–	–	–	–	–	–	–	
(0xD2)	Reserved	–	–	–	–	–	–	–	–	
(0xD1)	Reserved	–	–	–	–	–	–	–	–	
(0xD0)	Reserved	–	–	–	–	–	–	–	–	
(0xCF)	Reserved	–	–	–	–	–	–	–	–	
(0xCE)	Reserved	–	–	–	–	–	–	–	–	
(0xCD)	Reserved	–	–	–	–	–	–	–	–	
(0xCC)	Reserved	–	–	–	–	–	–	–	–	
(0xCB)	Reserved	–	–	–	–	–	–	–	–	
(0xCA)	Reserved	–	–	–	–	–	–	–	–	
(0xC9)	Reserved	–	–	–	–	–	–	–	–	
(0xC8)	Reserved	–	–	–	–	–	–	–	–	
(0xC7)	Reserved	–	–	–	–	–	–	–	–	
(0xC6)	UDR	USART I/O Data Register								170
(0xC5)	UBRRH					USART Baud Rate Register High				174
(0xC4)	UBRRL	USART Baud Rate Register Low								174
(0xC3)	Reserved	–	–	–	–	–	–	–	–	
(0xC2)	UCSRC	–	UMSEL	UPM1	UPM0	USBS	UCSZ1	UCSZ0	UCPOL	170
(0xC1)	UCSRB	RXCIE	TXCIE	UDRIE	RXEN	TXEN	UCSZ2	RXB8	TXB8	170
(0xC0)	UCSRA	RXC	TXC	UDRE	FE	DOR	UPE	U2X	MPCM	170

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0xBF)	Reserved	–	–	–	–	–	–	–	–	
(0xBE)	Reserved	–	–	–	–	–	–	–	–	
(0xBD)	Reserved	–	–	–	–	–	–	–	–	
(0xBC)	Reserved	–	–	–	–	–	–	–	–	
(0xBB)	Reserved	–	–	–	–	–	–	–	–	
(0xBA)	USIDR	USI Data Register								185
(0xB9)	USISR	USISIF	USIOIF	USIPF	USIDC	USICNT3	USICNT2	USICNT1	USICNT0	186
(0xB8)	USICR	USISIE	USIOIE	USIWM1	USIWM0	USICS1	USICS0	USICLK	USITC	187
(0xB7)	Reserved	–		–	–	–	–	–	–	
(0xB6)	ASSR	–	–	–	EXCLK	AS2	TCN2UB	OCR2UB	TCR2UB	138
(0xB5)	Reserved	–	–	–	–	–	–	–	–	
(0xB4)	Reserved	–	–	–	–	–	–	–	–	
(0xB3)	OCR2A	Timer/Counter2 Output Compare Register A								137
(0xB2)	TCNT2	Timer/Counter2 (8-bit)								137
(0xB1)	Reserved	–	–	–	–	–	–	–	–	
(0xB0)	TCCR2A	FOC2A	WGM20	COM2A1	COM2A0	WGM21	CS22	CS21	CS20	135
(0xAF)	Reserved	–	–	–	–	–	–	–	–	
(0xAE)	Reserved	–	–	–	–	–	–	–	–	
(0xAD)	Reserved	–	–	–	–	–	–	–	–	
(0xAC)	Reserved	–	–	–	–	–	–	–	–	
(0xAB)	Reserved	–	–	–	–	–	–	–	–	
(0xAA)	Reserved	–	–	–	–	–	–	–	–	
(0xA9)	Reserved	–	–	–	–	–	–	–	–	
(0xA8)	Reserved	–	–	–	–	–	–	–	–	
(0xA7)	Reserved	–	–	–	–	–	–	–	–	
(0xA6)	Reserved	–	–	–	–	–	–	–	–	
(0xA5)	Reserved	–	–	–	–	–	–	–	–	
(0xA4)	Reserved	–	–	–	–	–	–	–	–	
(0xA3)	Reserved	–	–	–	–	–	–	–	–	
(0xA2)	Reserved	–	–	–	–	–	–	–	–	
(0xA1)	Reserved	–	–	–	–	–	–	–	–	
(0xA0)	Reserved	–	–	–	–	–	–	–	–	
(0x9F)	Reserved	–	–	–	–	–	–	–	–	
(0x9E)	Reserved	–	–	–	–	–	–	–	–	
(0x9D)	Reserved	–	–	–	–	–	–	–	–	
(0x9C)	Reserved	–	–	–	–	–	–	–	–	
(0x9B)	Reserved	–	–	–	–	–	–	–	–	
(0x9A)	Reserved	–	–	–	–	–	–	–	–	
(0x99)	Reserved	–	–	–	–	–	–	–	–	
(0x98)	Reserved	–	–	–	–	–	–	–	–	
(0x97)	Reserved	–	–	–	–	–	–	–	–	
(0x96)	Reserved	–	–	–	–	–	–	–	–	
(0x95)	Reserved	–	–	–	–	–	–	–	–	
(0x94)	Reserved	–	–	–	–	–	–	–	–	
(0x93)	Reserved	–	–	–	–	–	–	–	–	
(0x92)	Reserved	–	–	–	–	–	–	–	–	
(0x91)	Reserved	–	–	–	–	–	–	–	–	
(0x90)	Reserved	–	–	–	–	–	–	–	–	
(0x8F)	Reserved	–	–	–	–	–	–	–	–	
(0x8E)	Reserved	–	–	–	–	–	–	–	–	
(0x8D)	Reserved	–	–	–	–	–	–	–	–	
(0x8C)	Reserved	–	–	–	–	–	–	–	–	
(0x8B)	OCR1BH	Timer/Counter1 - Output Compare Register B High Byte								121
(0x8A)	OCR1BL	Timer/Counter1 - Output Compare Register B Low Byte								121
(0x89)	OCR1AH	Timer/Counter1 - Output Compare Register A High Byte								121
(0x88)	OCR1AL	Timer/Counter1 - Output Compare Register A Low Byte								121
(0x87)	ICR1H	Timer/Counter1 - Input Capture Register High Byte								122
(0x86)	ICR1L	Timer/Counter1 - Input Capture Register Low Byte								122
(0x85)	TCNT1H	Timer/Counter1 - Counter Register High Byte								121
(0x84)	TCNT1L	Timer/Counter1 - Counter Register Low Byte								121
(0x83)	Reserved	–	–	–	–	–	–	–	–	
(0x82)	TCCR1C	FOC1A	FOC1B	–	–	–	–	–	–	120
(0x81)	TCCR1B	ICNC1	ICES1	–	WGM13	WGM12	CS12	CS11	CS10	119
(0x80)	TCCR1A	COM1A1	COM1A0	COM1B1	COM1B0	–	–	WGM11	WGM10	117
(0x7F)	DIDR1	–	–	–	–	–	–	AIN1D	AIN0D	192
(0x7E)	DIDR0	ADC7D	ADC6D	ADC5D	ADC4D	ADC3D	ADC2D	ADC1D	ADC0D	209

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
(0x7D)	Reserved	–	–	–	–	–	–	–	–	
(0x7C)	ADMUX	REFS1	REFS0	ADLAR	MUX4	MUX3	MUX2	MUX1	MUX0	205
(0x7B)	ADCSRB	–	ACME	–	–	–	ADTS2	ADTS1	ADTS0	190, 209
(0x7A)	ADCSRA	ADEN	ADSC	ADATE	ADIF	ADIE	ADPS2	ADPS1	ADPS0	207
(0x79)	ADCH	ADC Data Register High byte								208
(0x78)	ADCL	ADC Data Register Low byte								208
(0x77)	Reserved	–	–	–	–	–	–	–	–	
(0x76)	Reserved	–	–	–	–	–	–	–	–	
(0x75)	Reserved	–	–	–	–	–	–	–	–	
(0x74)	Reserved	–	–	–	–	–	–	–	–	
(0x73)	Reserved	–	–	–	–	–	–	–	–	
(0x72)	Reserved	–	–	–	–	–	–	–	–	
(0x71)	Reserved	–	–	–	–	–	–	–	–	
(0x70)	TIMSK2	–	–	–	–	–	–	OCIE2A	TOIE2	140
(0x6F)	TIMSK1	–	–	ICIE1	–	–	OCIE1B	OCIE1A	TOIE1	122
(0x6E)	TIMSK0	–	–	–	–	–	–	OCIE0A	TOIE0	92
(0x6D)	Reserved	–	–	–	–	–	–	–	–	
(0x6C)	PCMSK1	PCINT15	PCINT14	PCINT13	PCINT12	PCINT11	PCINT10	PCINT9	PCINT8	54
(0x6B)	PCMSK0	PCINT7	PCINT6	PCINT5	PCINT4	PCINT3	PCINT2	PCINT1	PCINT0	54
(0x6A)	Reserved	–	–	–	–	–	–	–	–	
(0x69)	EICRA	–	–	–	–	–	–	ISC01	ISC00	52
(0x68)	Reserved	–	–	–	–	–	–	–	–	
(0x67)	Reserved	–	–	–	–	–	–	–	–	
(0x66)	OSCCAL	Oscillator Calibration Register								28
(0x65)	Reserved	–	–	–	–	–	–	–	–	
(0x64)	PRR	–	–	–	PRLCD	PRTIM1	PRSPI	PRUSART0	PRADC	34
(0x63)	Reserved	–	–	–	–	–	–	–	–	
(0x62)	Reserved	–	–	–	–	–	–	–	–	
(0x61)	CLKPR	CLKPCE	–	–	–	CLKPS3	CLKPS2	CLKPS1	CLKPS0	30
(0x60)	WDTCR	–	–	–	WDCE	WDE	WDP2	WDP1	WDP0	43
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0x3E (0x5E)	SPH	–	–	–	–	–	SP10	SP9	SP8	11
0x3D (0x5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	11
0x3C (0x5C)	Reserved									
0x3B (0x5B)	Reserved									
0x3A (0x5A)	Reserved									
0x39 (0x59)	Reserved									
0x38 (0x58)	Reserved									
0x37 (0x57)	SPMCSR	SPMIE	RWWSB	–	RWWSRE	BLBSET	PGWRT	PGERS	SPMEN	257
0x36 (0x56)	Reserved	–	–	–	–	–	–	–	–	
0x35 (0x55)	MCUCR	JTD	–	–	PUD	–	–	IVSEL	IVCE	235
0x34 (0x54)	MCUSR	–	–	–	JTRF	WDRF	BORF	EXTRF	PORF	236
0x33 (0x53)	SMCR	–	–	–	–	SM2	SM1	SM0	SE	32
0x32 (0x52)	Reserved	–	–	–	–	–	–	–	–	
0x31 (0x51)	OCDR	IDRD/OCD	OCDR6	OCDR5	OCDR4	OCDR3	OCDR2	OCDR1	OCDR0	231
0x30 (0x50)	ACSR	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0	190
0x2F (0x4F)	Reserved	–	–	–	–	–	–	–	–	
0x2E (0x4E)	SPDR	SPI Data Register								150
0x2D (0x4D)	SPSR	SPIF	WCOL	–	–	–	–	–	SPI2X	150
0x2C (0x4C)	SPCR	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	148
0x2B (0x4B)	GPIOR2	General Purpose I/O Register 2								22
0x2A (0x4A)	GPIOR1	General Purpose I/O Register 1								22
0x29 (0x49)	Reserved	–	–	–	–	–	–	–	–	
0x28 (0x48)	Reserved	–	–	–	–	–	–	–	–	
0x27 (0x47)	OCR0A	Timer/Counter0 Output Compare Register A								92
0x26 (0x46)	TCNT0	Timer/Counter0 (8 Bit)								91
0x25 (0x45)	Reserved	–	–	–	–	–	–	–	–	
0x24 (0x44)	TCCR0A	FOC0A	WGM00	COM0A1	COM0A0	WGM01	CS02	CS01	CS00	89
0x23 (0x43)	GTCCR	TSM	–	–	–	–	–	PSR2	PSR10	94
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0x1C (0x3C)	EIFR	PCIF1	PCIF0	–	–	–	–	–	INTF0	53

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
0x1B (0x3B)	Reserved	–	–	–	–	–	–	–	–	
0x1A (0x3A)	Reserved	–	–	–	–	–	–	–	–	
0x19 (0x39)	Reserved	–	–	–	–	–	–	–	–	
0x18 (0x38)	Reserved	–	–	–	–	–	–	–	–	
0x17 (0x37)	TIFR2	–	–	–	–	–	–	OCF2A	TOV2	141
0x16 (0x36)	TIFR1	–	–	ICF1	–	–	OCF1B	OCF1A	TOV1	123
0x15 (0x35)	TIFR0	–	–	–	–	–	–	OCF0A	TOV0	92
0x14 (0x34)	PORTG	–	–	–	PORTG4	PORTG3	PORTG2	PORTG1	PORTG0	78
0x13 (0x33)	DDRG	–	–	–	DDG4	DDG3	DDG2	DDG1	DDG0	78
0x12 (0x32)	PING	–	–	–	PING4	PING3	PING2	PING1	PING0	78
0x11 (0x31)	PORTF	PORTF7	PORTF6	PORTF5	PORTF4	PORTF3	PORTF2	PORTF1	PORTF0	77
0x10 (0x30)	DDRF	DDF7	DDF6	DDF5	DDF4	DDF3	DDF2	DDF1	DDF0	77
0x0F (0x2F)	PINF	PINF7	PINF6	PINF5	PINF4	PINF3	PINF2	PINF1	PINF0	78
0x0E (0x2E)	PORTE	PORTE7	PORTE6	PORTE5	PORTE4	PORTE3	PORTE2	PORTE1	PORTE0	77
0x0D (0x2D)	DDRE	DDE7	DDE6	DDE5	DDE4	DDE3	DDE2	DDE1	DDE0	77
0x0C (0x2C)	PINE	PINE7	PINE6	PINE5	PINE4	PINE3	PINE2	PINE1	PINE0	77
0x0B (0x2B)	PORTD	PORTD7	PORTD6	PORTD5	PORTD4	PORTD3	PORTD2	PORTD1	PORTD0	77
0x0A (0x2A)	DDRD	DDD7	DDD6	DDD5	DDD4	DDD3	DDD2	DDD1	DDD0	77
0x09 (0x29)	PIND	PIND7	PIND6	PIND5	PIND4	PIND3	PIND2	PIND1	PIND0	77
0x08 (0x28)	PORTC	PORTC7	PORTC6	PORTC5	PORTC4	PORTC3	PORTC2	PORTC1	PORTC0	76
0x07 (0x27)	DDRC	DDC7	DDC6	DDC5	DDC4	DDC3	DDC2	DDC1	DDC0	76
0x06 (0x26)	PINC	PINC7	PINC6	PINC5	PINC4	PINC3	PINC2	PINC1	PINC0	77
0x05 (0x25)	PORTB	PORTB7	PORTB6	PORTB5	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	76
0x04 (0x24)	DDRB	DDB7	DDB6	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	76
0x03 (0x23)	PINB	PINB7	PINB6	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	76
0x02 (0x22)	PORTA	PORTA7	PORTA6	PORTA5	PORTA4	PORTA3	PORTA2	PORTA1	PORTA0	76
0x01 (0x21)	DDRA	DDA7	DDA6	DDA5	DDA4	DDA3	DDA2	DDA1	DDA0	76
0x00 (0x20)	PINA	PINA7	PINA6	PINA5	PINA4	PINA3	PINA2	PINA1	PINA0	76

Note: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the Status Flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such Status Flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses. The ATmega169 is a complex microcontroller with more peripheral units than can be supported within the 64 location reserved in Opcode for the IN and OUT instructions. For the Extended I/O space from 0x60 - 0xFF in SRAM, only the ST/STS/STD and LD/LDS/LDD instructions can be used.

Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clocks
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd - Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd - K	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd - Rr - C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd - K - C	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl - K	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← 0xFF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← 0x00 – Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • (0xFF - K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd – 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← 0xFF	None	1
MUL	Rd, Rr	Multiply Unsigned	R1:R0 ← Rd x Rr	Z,C	2
MULS	Rd, Rr	Multiply Signed	R1:R0 ← Rd x Rr	Z,C	2
MULSU	Rd, Rr	Multiply Signed with Unsigned	R1:R0 ← Rd x Rr	Z,C	2
FMUL	Rd, Rr	Fractional Multiply Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULS	Rd, Rr	Fractional Multiply Signed	R1:R0 ← (Rd x Rr) << 1	Z,C	2
FMULSU	Rd, Rr	Fractional Multiply Signed with Unsigned	R1:R0 ← (Rd x Rr) << 1	Z,C	2
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
JMP	k	Direct Jump	PC ← k	None	3
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
CALL	k	Direct Subroutine Call	PC ← k	None	4
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b)=1) PC ← PC + 2 or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC+k + 1	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC+k + 1	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1/2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1/2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1/2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1/2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1/2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow.	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
MOVW	Rd, Rr	Copy Register Word	Rd+1:Rd ← Rr+1:Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
LPM	Rd, Z	Load Program Memory	Rd ← (Z)	None	3
LPM	Rd, Z+	Load Program Memory and Post-Inc	Rd ← (Z), Z ← Z+1	None	3
SPM		Store Program Memory	(Z) ← R1:R0	None	-
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2

Mnemonics	Operands	Description	Operation	Flags	#Clocks
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
MCU CONTROL INSTRUCTIONS					
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep function)	None	1
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1
BREAK		Break	For On-chip Debug Only	None	N/A

Ordering Information

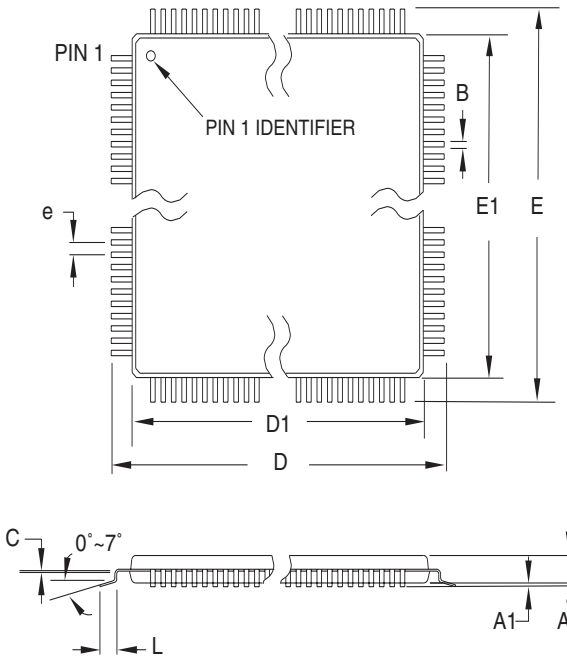
Speed (MHz)[3]	Power Supply	Ordering Code	Package[1]	Operation Range
8	1.8 - 5.5V	ATmega169V-8AI ATmega169V-8AU[2] ATmega169V-8MI ATmega169V-8MU[2]	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)
16	2.7 - 5.5V	ATmega169-16AI ATmega169-16AU[2] ATmega169-16MI ATmega169-16MU[2]	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC}, see Figure 136 on page 301 and Figure 137 on page 301.

Package Type	
64A	64-Lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)
64M1	64-pad, 9 x 9 x 1.0 mm body, lead pitch 0.50 mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

Packaging Information

64A



COMMON DIMENSIONS
(Unit of Measure = mm)

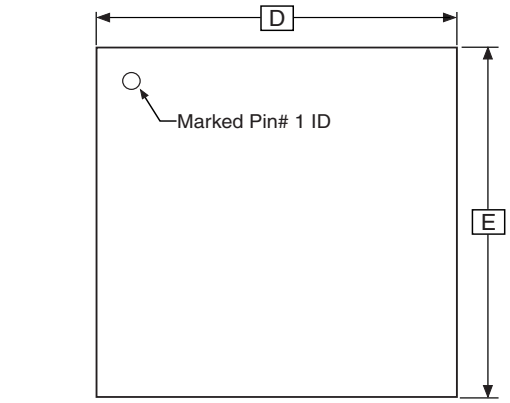
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

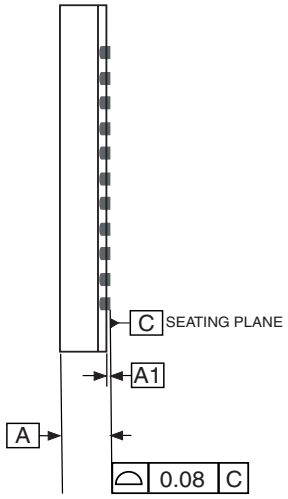
10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**64A,** 64-lead, 14 x 14 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	64A	B

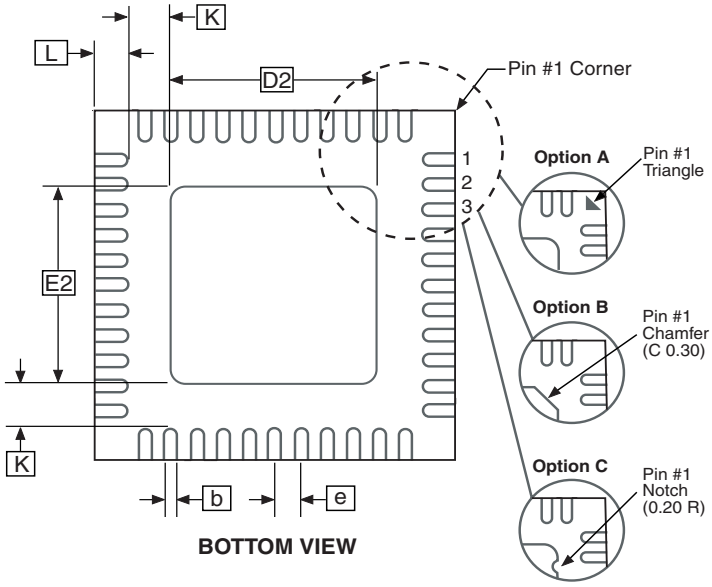
64M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	5.20	5.40	5.60	
E	8.90	9.00	9.10	
E2	5.20	5.40	5.60	
e		0.50 BSC		
L	0.35	0.40	0.45	
K	1.25	1.40	1.55	

Note: 1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

5/25/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**64M1**, 64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.40 mm Exposed Pad, Micro Lead Frame Package (MLF)	64M1	G

Errata

ATmega169 Rev E

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. Interrupts may be lost when writing the timer registers in the asynchronous timer

If one of the timer registers which is synchronized to the asynchronous timer2 clock is written in the cycle before a overflow interrupt occurs, the interrupt may be lost.

Problem Fix/Workaround

Always check that the Timer2 Timer/Counter register, TCNT2, does not have the value 0xFF before writing the Timer2 Control Register, TCCR2, or Output Compare Register, OCR2.

ATmega169 Rev D

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **High serial resistance in the glass can result in dim segments on the LCD**
- **IDCODE masks data from TDI input**

3. Interrupts may be lost when writing the timer registers in the asynchronous timer

If one of the timer registers which is synchronized to the asynchronous timer2 clock is written in the cycle before a overflow interrupt occurs, the interrupt may be lost.

Problem Fix/Workaround

Always check that the Timer2 Timer/Counter register, TCNT2, does not have the value 0xFF before writing the Timer2 Control Register, TCCR2, or Output Compare Register, OCR2.

2. High serial resistance in the glass can result in dim segments on the LCD

Some display types with high serial resistance (>20 kΩ) inside the glass can result in dim segments on the LCD

Problem Fix/Workaround

Add a 1 nF (0.47 - 1.5 nF) capacitor between each common pin and ground.

1. IDCODE masks data from TDI input

The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

Problem Fix / Workaround

– If ATmega169 is the only device in the scan chain, the problem is not visible.

– Select the Device ID Register of the ATmega169 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega169 while reading the Device ID Registers of preceding devices of the boundary scan chain.

– If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega169 must be the first device in the chain.

ATmega169 Rev C

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **High Current Consumption In Power Down when JTAGEN is Programmed**
- **LCD Contrast Control**
- **Some Data Combinations Can Result in Dim Segments on the LCD**
- **LCD Current Consumption**
- **IDCODE masks data from TDI input**

6. Interrupts may be lost when writing the timer registers in the asynchronous timer

If one of the timer registers which is synchronized to the asynchronous timer2 clock is written in the cycle before a overflow interrupt occurs, the interrupt may be lost.

Problem Fix/Workaround

Always check that the Timer2 Timer/Counter register, TCNT2, does not have the value 0xFF before writing the Timer2 Control Register, TCCR2, or Output Compare Register, OCR2.

5. High Current Consumption In Power Down when JTAGEN is Programmed

The input buffer on TDO (PF6) is always enabled and the pull-up is always disabled when JTAG is programmed. This can leave the output floating.

Problem Fix/Workaround

Add external pull-up to PF6.

Unprogram the JTAGEN Fuse before shipping out the end product.

4. LCD Contrast Control

The contrast control is not working properly when using synchronous clock (chip clock) to obtain an LCD clock, and the chip clock is 125 kHz or faster.

Problem Fix/Workaround

Use a low chip clock frequency (32 kHz) or apply an external voltage to the LCD-CAP pin.

3. Some Data Combinations Can Result in Dim Segments on the LCD

All segments connected to a common plane might be dimmed (lower contrast) when a certain combination of data is displayed.

Problem Fix/Workaround

Default waveform: If there are any unused segment pins, loading one of these with a 1 nF capacitor and always write ‘0’ to this segment eliminates the problem.

Low power waveform: Add a 1 nF capacitor to each common pin.

2. LCD Current Consumption

In an interval where V_{CC} is within the range VLCD -0.2V to VLCD + 0.4V, the LCD current consumption is up to three times higher than expected. This will only be an issue in Power-save mode with the LCD running as the LCD current is negligible compared to the overall power consumption in all other modes of operation.

Problem Fix/Workaround

No known workaround.

1. IDCODE masks data from TDI input

The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

Problem Fix / Workaround

– If ATmega169 is the only device in the scan chain, the problem is not visible.

– Select the Device ID Register of the ATmega169 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega169 while reading the Device ID Registers of preceding devices of the boundary scan chain.

– If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega169 must be the first device in the chain.

ATmega169 Rev B

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **Internal Oscillator Runs at 4 MHz**
- **LCD Contrast Voltage is not Correct**
- **External Oscillator is Non-functional**
- **USART**
- **ADC Measures with Lower Accuracy than Specified**
- **Serial Downloading**
- **IDCODE masks data from TDI input**

8. Interrupts may be lost when writing the timer registers in the asynchronous timer

If one of the timer registers which is synchronized to the asynchronous timer2 clock is written in the cycle before a overflow interrupt occurs, the interrupt may be lost.

Problem Fix/Workaround

Always check that the Timer2 Timer/Counter register, TCNT2, does not have the value 0xFF before writing the Timer2 Control Register, TCCR2, or Output Compare Register, OCR2.

7. Internal Oscillator Runs at 4 MHz

The Internal Oscillator runs at 4 MHz instead of the specified 8 MHz. Therefore, all Flash/EEPROM programming times are twice as long as specified. This includes Chip Erase, Byte programming, Page programming, Fuse programming, Lock bit programming, EEPROM write from the CPU, and Flash Self-Programming.

For this reason, rev-B samples are shipped with the CKDIV8 Fuse unprogrammed.

Problem Fix/Workaround

If 8 MHz operation is required, apply an external clock (this will be fixed in rev. C).

6. LCD Contrast Voltage is not Correct

The LCD contrast voltage between 1.8V and 3.1V is incorrect. When the V_{CC} is between 1.8V and 3.1V, the LCD contrast voltage drops approx. 0.5V. The current consumption in this interval is higher than expected.

Problem Fix/Workaround

Contrast will be wrong, but display will still be readable, can be partly compensated for using the contrast control register (this will be fixed in rev. C).

5. External Oscillator is Non-functional

The external oscillator does not run with the setup described in the datasheet.

Problem Fix/Workaround

Use other clock source (this will be fixed in rev. C).

Alternative Problem Fix/Workaround

Adding a pull-down on XTAL1 will start the Oscillator.

4. USART

Writing TXEN to zero during transmission causes the transmission to suddenly stop. The datasheet description tells that the transmission should complete before stopping the USART when TXEN is written to zero.

Problem Fix/Workaround

Ensure that the transmission is complete before writing TXEN to zero (this will be fixed in rev. C).

3. ADC Measures with Lower Accuracy than Specified

The ADC does not work as intended. There is a positive offset in the result.

Problem Fix/Workaround

This will be fixed in rev. C.

2. Serial downloading

When entering Serial Programming mode the second byte will not echo back as described in the Serial Programming algorithm.

Problem Fix/Workaround

Check if the third byte echoes back to ensure that the device is in Programming mode (this will be fixed in rev. C).

1. IDCODE masks data from TDI input

The JTAG instruction IDCODE is not working correctly. Data to succeeding devices are replaced by all-ones during Update-DR.

Problem Fix / Workaround

– If ATmega169 is the only device in the scan chain, the problem is not visible.

– Select the Device ID Register of the ATmega169 by issuing the IDCODE instruction or by entering the Test-Logic-Reset state of the TAP controller to read out the contents of its Device ID Register and possibly data from succeeding devices of the scan chain. Issue the BYPASS instruction to the ATmega169 while reading the Device ID Registers of preceding devices of the boundary scan chain.

– If the Device IDs of all devices in the boundary scan chain must be captured simultaneously, the ATmega169 must be the first device in the chain.

Datasheet Revision History

Please note that the referring page numbers in this section are referring to this document. The referring revision in this section are referring to the document revision.

Changes from Rev. 2514O-03/06 to Rev. 2514P-07/06

1. Updated “Fast PWM Mode” on page 109.
2. Updated Features in “USI – Universal Serial Interface” on page 179.
3. Added “Clock speed considerations.” on page 185.
4. Updated “Bit 6 – ACBG: Analog Comparator Bandgap Select” on page 191.
5. Updated Table 49 on page 90, Table 51 on page 90, Table 56 on page 117, Table 57 on page 118, Table 58 on page 119, Table 61 on page 135 and Table 63 on page 136.
6. Updated “Prescaling and Conversion Timing” on page 196.
7. Updated Features in “LCD Controller” on page 210.
8. Updated “Errata” on page 349.

Changes from Rev. 2514N-03/06 to Rev. 2514O-03/06

1. Updated number of General purpose I/O pins from 53 to 54.
2. Updated “Serial Peripheral Interface – SPI” on page 143.

Changes from Rev. 2514M-05/05 to Rev. 2514N-03/06

1. Added Not recommended in new designs.
2. Removed the notice: This datasheet covers revision A to E of ATmega169. Revision F and onwards are now covered in ATmega169 datasheet, “doc2597.pdf” found on www.atmel.com/avr.
3. Updated Table 17 on page 40.

Changes from Rev. 2514L-03/05 to Rev. 2514M-05/05

1. This datasheet covers revision A to E of ATmega169.
   Revision F and onwards are now covered in ATmega169 datasheet, “doc2597.pdf” found on www.atmel.com/avr.

Changes from Rev. 2514K-04/04 to Rev. 2514L-03/05

1. MLF-package alternative changed to “Quad Flat No-Lead/Micro Lead Frame Package QFN/MLF”.
2. Updated Table 16 on page 38, Table 56 on page 117, Table 57 on page 118, Table 98 on page 223, Table 99 on page 223, Table 100 on page 224 and Table 130 on page 284.
3. Added “Pin Change Interrupt Timing” on page 51.
4. Updated C Code Example in “USART Initialization” on page 157.
5. Added note to “Power Reduction Register - PRR” on page 34 and “LCD Contrast Control Register – LCDCCR” on page 223.
6. Moved “No. of Words in a Page and No. of Pages in the Flash” and “No. of Words in a Page and No. of Pages in the EEPROM” to “Page Size” on page 269.
7. Updated “Serial Programming Algorithm” on page 282.
8. Updated “ATmega169 Typical Characteristics” on page 305.

9. Renamed “Using the Power Reduction Register” to “Supply Current of I/O modules” on page 310.
10. Updated “Register Summary” on page 339.
11. Updated “Ordering Information” on page 346.
12. Updated Figure 83 on page 194, Figure 91 on page 201, and Figure 123 on page 277.

Changes from Rev. 2514J-12/03 to Rev. 2514K-04/04

1. Changed size from 0x60 to 0xFF in “Stack Pointer” on page 11.
2. Updated Table 17 on page 40, Table 21 on page 44 and Table 115 on page 265.
3. Updated “Calibrated Internal RC Oscillator” on page 27.
4. Added new “Power Reduction Register” on page 34.
   Examples found in “Supply Current of I/O modules” on page 310.
5. Fixed typo in port description for the “Analog to Digital Converter” on page 193.
6. Removed old and added new “LCD Controller” on page 210.
7. Updated “Electrical Characteristics” on page 298.
8. Updated “ATmega169 Typical Characteristics” on page 305.
9. Updated “Ordering Information” on page 346.
   ATmega169L replaced by ATmega169V and ATmega169.

Changes from Rev. 2514I-09/03 to Rev. 2514J-12/03

1. Updated “Calibrated Internal RC Oscillator” on page 27

Changes from Rev. 2514H-05/03 to Rev. 2514I-09/03

1. Removed “Advance Information” from the datasheet.
2. Removed AGND from Figure 2 on page 3 and added “System Clock Prescaler” to Figure 11 on page 23.
3. Updated Table 16 on page 38, Table 17 on page 40, Table 19 on page 42 and Table 41 on page 72.
4. Renamed and updated “On-chip Debug System” to “JTAG Interface and On-chip Debug System” on page 36.
5. Updated COM01:0 to COM0A1:0 in “Timer/Counter Control Register A – TCCR0A” on page 89 and COM21:0 to COM2A1:0 in “Timer/Counter Control Register A– TCCR2A” on page 135.
6. Updated “Test Access Port – TAP” on page 226 regarding JTAGEN.
7. Updated description for the JTD bit on page 235.
8. Added a note regarding JTAGEN fuse to Table 119 on page 268.
9. Updated Absolute Maximum Ratings* and DC Characteristics in “Electrical Characteristics” on page 298.
10. Updated “Errata” on page 349 and added a proposal for solving problems regarding the JTAG instruction IDCODE.

Changes from Rev. 2514G-04/03 to Rev. 2514H-05/03

1. Updated typo in Figure 148, Figure 168, and Figure 195.

Changes from Rev. 2514F-04/03 to Rev. 2514G-04/03

1. Updated “ATmega169 Typical Characteristics” on page 305.
2. Updated typo in “Ordering Information” on page 346.
3. Updated Figure 46 on page 109, Table 18 on page 40, and “Version” on page 233.

Changes from Rev. 2514E-02/03 to Rev. 2514F-04/03

1. Renamed ICP to ICP1 in whole document.
2. Removed note on “Crystal Oscillator Operating Modes” on page 25.
3. XTAL1/XTAL2 can be used as timer oscillator pins, described in chapter “Calibrated Internal RC Oscillator” on page 27.
4. Switching between prescaler settings in “System Clock Prescaler” on page 29.
5. Updated DC and ACD Characteristics in chapter “Electrical Characteristics” on page 298 are updated. Removed TBD’s from Table 16 on page 38, Table 19 on page 42, Table 134 on page 301.
6. Updated Figure 23 on page 56, Figure 26 on page 60 and Figure 110 on page 238 regarding WRITE PINx REGISTER.
7. Updated “Alternate Functions of Port F” on page 72 regarding JTAG.
8. Replaced Timer0 Overflow with Timer/Counter0 Compare Match in “USI – Universal Serial Interface” on page 179. Also updated “Start Condition Detector” on page 185 and “USI Control Register – USICR” on page 187.
9. Updated Features for “Analog to Digital Converter” on page 193 and Table 88 on page 205.
10. Added notes on Figure 118 on page 259 and Table 118 on page 267.

Changes from Rev. 2514D-01/03 to Rev. 2514E-02/03

1. Updated the section “Features” on page 1 with information regarding ATmega169 and ATmega169L.
2. Removed all references to the PG5 pin in Figure 1 on page 2, Figure 2 on page 3, “Port G (PG4..PG0)” on page 6, “Alternate Functions of Port G” on page 74, and “Register Description for I/O-Ports” on page 76.
3. Updated Table 118, “Extended Fuse Byte,” on page 267.
4. Added Errata for “Datasheet Revision History” on page 353, including “Significant Data Sheet Changes”.

5. Updated the “Ordering Information” on page 346 to include the new speed grade for ATmega169L and the new 16 MHz ATmega169.

Changes from Rev. 2514C-11/02 to Rev. 2514D-01/03

1. Added TCK frequency limit in “Programming via the JTAG Interface” on page 285.
2. Added Chip Erase as a first step in “Programming the Flash” on page 295 and “Programming the EEPROM” on page 296.
3. Added the section “Unconnected Pins” on page 60.
4. Added tips on how to disable the OCD system in “On-chip Debug System” on page 35.
5. Corrected interrupt addresses. ADC and ANA_COMP had swapped places.
6. Improved the table in “SPI Timing Characteristics” on page 301 and removed the table in “SPI Serial Programming Characteristics” on page 285.
7. Changed “will be ignored” to “must be written to zero” for unused Z-pointer bits in “Performing a Page Write” on page 260.
8. Corrected “LCD Frame Complete” to “LCD Start of Frame” in the LCDCRA Register description.
9. Changed OUT to STS and IN to LDS in USI code examples, and corrected f_{SCKmax}. The USI I/O Registers are in the extended I/O space, so IN and OUT cannot be used. LDS and STS take one more cycle when executed, so f_{SCKmax} had to be changed accordingly.
10. Removed TOSKON and TOSCK from Table 103 on page 239, and g10 and g20 from Figure 115 on page 241 and Table 105 on page 242, because these signals do not exist in boundary scan.
11. Changed from 4 to 16 MIPS and MHz in the device Features list.
12. Corrected Port A to Port F in “AVCC” on page 6 under “Pin Descriptions” on page 5.
13. Corrected 230.4 Mbps to 230.4 kbps in “Examples of Baud Rate Setting” on page 175.
14. Corrected placing of falling and rising XCK edges in Table 78, “UCPOL Bit Settings,” on page 174.
15. Removed reference to Multipurpose Oscillator Application Note, which does not exist.
16. Corrected Number of Calibrated RC Oscillator Cycles in Table 1 on page 19 from 8,448 to 67,584.
17. Various minor Timer1 corrections.

18. Added information about PWM symmetry for Timer0 and Timer2.
19. Corrected the contents of DIDR0 and DIDR1.
20. Made all bit names in the LCDDR Registers unique by adding the COM number digit in front of the two digits already there, e.g. SEG304.
21. Changed Extended Standby to ADC Noise Reduction mode under “Asynchronous Operation of Timer/Counter2” on page 139.
22. Added note about Port B having better driving capabilities than the other ports. As a consequence the table, “DC Characteristics” on page 298 was corrected as well.
23. Added note under “Filling the Temporary Buffer (Page Loading)” on page 260 about writing to the EEPROM during an SPM page load.
24. Removed ADHSM completely.
25. Updated “Packaging Information” on page 347.

Changes from Rev. 2514B-09/02 to Rev. 2514C-11/02

1. Added “Errata” on page 349.
2. Added Information for the 64-pad MLF Package in “Ordering Information” on page 346 and “Packaging Information” on page 347.
3. Changed Temperature Range and Removed Industrial Ordering Codes in “Packaging Information” on page 347.

Changes from Rev. 2514A-08/02 to Rev. 2514B-09/02

1. Changed the Endurance on the Flash to 10,000 Write/Erase Cycles.

Table of Contents

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